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VITESSE
SEMICONDUCTOR CORPORATION

1991 Product Data Book

VITESSE *Semiconductor Corporation*

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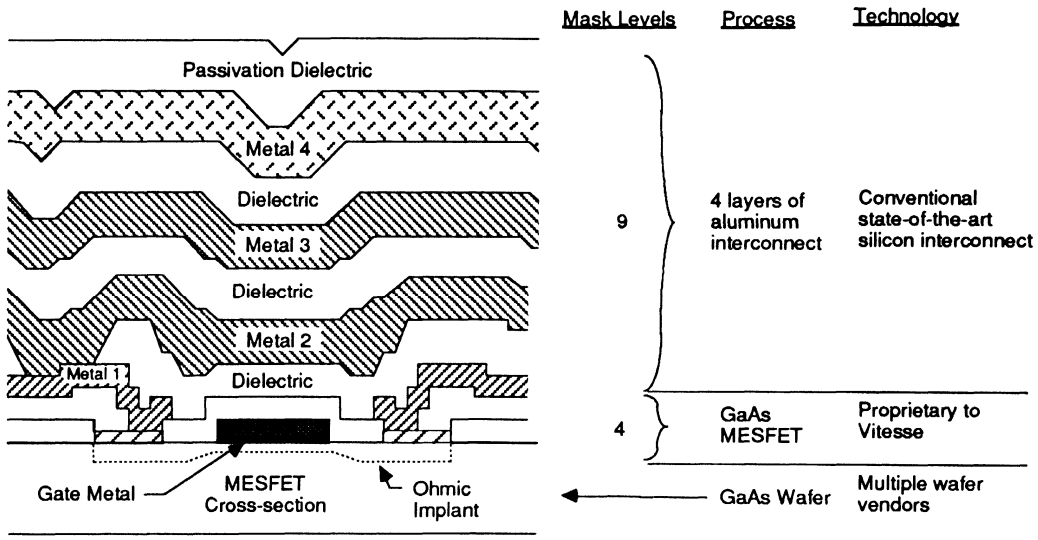
Introduction to the 1991 Product Data Book

This 1991 Product Data Book contains the latest information on the entire range of products and services from Vitesse Semiconductor Corporation. We are pleased to present you with this compilation of information in one convenient source. This book includes complete product data sheets for all standard products, gate arrays, standard cells, and foundry services. Supplementary information regarding packaging, applications, quality assurance and reliability is also included.

Vitesse Semiconductor Corporation is a proven leader in the design and manufacture of high performance digital LSI and VLSI GaAs ICs. The company, which was founded in 1984, has developed a revolutionary new process, allowing it to deliver the first affordable very large scale integrated circuits (VLSI) in gallium arsenide (GaAs). With the introduction of the FURY Gate Array family in 1988, Vitesse became the first company to deliver VLSI GaAs circuits into production systems. Now in 1991, Vitesse has complemented its VLSI offerings with the introduction of the FX Gate Array family with integration reaching 350,000 gates.

The key to success for Vitesse has been the development of its unique H-GaAs manufacturing technology. Rather than developing a process based on existing GaAs microwave transistor technology as others in the GaAs industry had done, Vitesse chose to develop an entirely new process based on proven silicon MOS manufacturing methods. This strategy solved two major problems which had prevented GaAs ICs from receiving wide acceptance: low complexity and high cost. The result is a high yielding, proprietary process which produces circuits with a speed-power product unmatched by any other IC manufacturing technology.



The market for Vitesse's products is existing high performance silicon users. In order to compete in this marketplace, Vitesse chose to make its products look and feel exactly like silicon products, but with significant improvements in speed, complexity, and reduced power dissipation. The combination of GaAs performance and silicon MOS manufacturing techniques is the key Vitesse advantage. The results are families of IC products that set new performance standards at prices equal to high performance silicon bipolar products and provide equal price/performance ratios to BiCMOS products.

Vitesse is committed to providing the highest performance integrated circuits in the world. Vitesse products have surpassed silicon ECL products in terms of performance and complexity, all at a lower price. Our next objective is to introduce an alternative to BiCMOS which provides equivalent complexity at far superior performance. The Vitesse manufacturing process has been designed to realize this objective with a combination of process innovations and proven MOS manufacturing techniques. The distinguishing features of the Vitesse process are: 1) excellent transistor electrical parameter control, 2) unprecedented manufacturing yields on VLSI complexity GaAs circuits, and 3) process simplicity and fast cycle time.

Vitesse has pioneered the now well-accepted concept of designing GaAs products that are compatible with existing silicon technologies. Input/output levels and power supplies found in TTL, ECL and CMOS are standard in the entire family of Vitesse products. In addition, standard ASIC (application specific IC) design tools allow designers to implement their circuits in a Vitesse gate array or cell based product exactly as they would with conventional silicon ASIC products. Synthesis tools, such as Synopsys™, are supported and facilitate retargetting a silicon design into GaAs technology with a minimum of effort and risk.

MEMORY

In addition to embedded RAM and register file capability in our ASIC products, Vitesse also offers several stand-alone RAM products. These products range in complexity from 1Kbits to 16Kbits. Some specialized functions, such as fast purging and self-timed or registered operation, are also available.

TELECOMMUNICATIONS

The family of telecommunications ICs from Vitesse are designed to address the needs of the newest generation of telecommunications systems incorporating data rates up to 2.5 Gigabits per second. These standard multiplexers and demultiplexers are available in 4, 8 and 12 channel configurations. These products feature very low power dissipation and ECL compatibility. The 8-channel mux/demux products are compatible with the Synchronous Optical Network (SONET) protocol for digital optical transmission. In addition, a 64 x 64 crosspoint chip capable of 200 Mb/s operation is available.

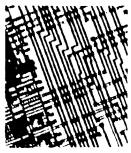
SEMICUSTOM PRODUCTS

Vitesse offers four families of gate arrays in addition to our standard cell library. The gate array families include: the FX series, the FURY series, the PLR2KT array, and the HS series. The FX series offers unparalleled complexity and performance in a channeless array architecture. The FURY series features a balance between speed and power, which offers performance equal to or better than the best ECL bipolar technologies with only a fraction of the power dissipation. Vitesse arrays come in many convenient sizes ranging from 1500 to 350,000 gates. The FX and FURY families offer TTL, ECL or native GaAs signal interface for maximum flexibility. The HS series, made up of two arrays, feature a structured cell approach which combines very high speed source coupled FET logic (SCFL), with very low power direct coupled FET logic (DCFL) for maximum speed/power flexibility. The HS arrays, both sized at 1500 gates, feature ECL I/O interface and can handle data rates up to 2.5GHz.

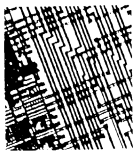
The VCB50K Standard Cell Library offers all of the flexibility of a full custom design without the long design cycle. This library features a complete offering of fully defined cells including complex function megacells, and RAM and ROM blocks. VCB50K Standard Cell designs are fully supported on the VLSI Technology Inc. tool set. All Vitesse semicustom products are fully supported with standard CAD platforms and software. All semicustom products offer commercial, industrial, or military operating temperature ranges.

FOUNDRY SERVICES

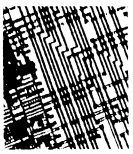
Vitesse has paved the way for designers wishing to realize their circuits in Gallium Arsenide by implementing a very simple, silicon-like MOS process. To this, enhancement/depletion (E/D) mode technology adds the flexibility of implementing a variety of logic families. Other important features of the process include: VLSI levels of complexity, self-aligned active devices, 0.6 micron minimum feature size, extended temperature range, resistance to ionizing radiation, and high yields. Vitesse offers an intensive three-day seminar to introduce the designer to digital GaAs IC design.



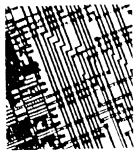
Section Index



Semicustom Product Index



Standard Product Index



Supplemental Information Index

Custom Products

Packaging

Application Notes

VITESSE

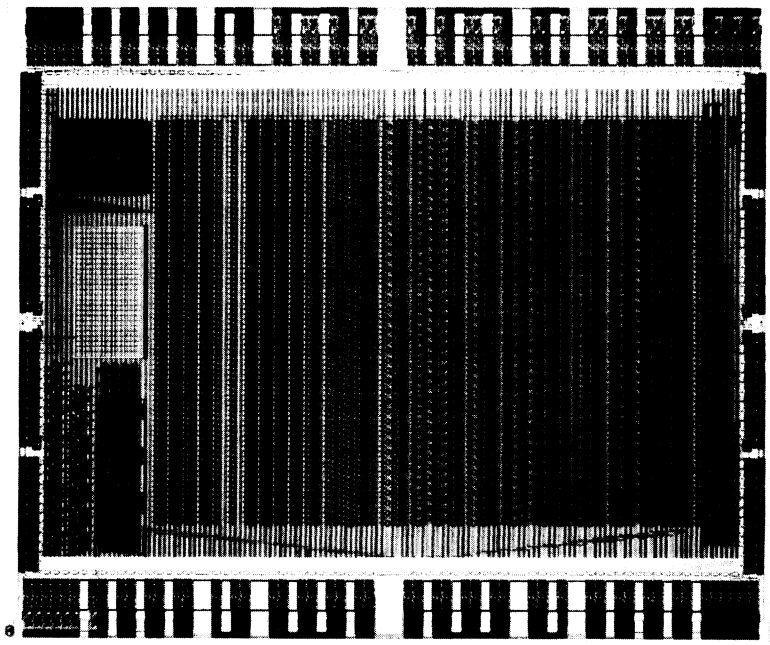
VGFX100K/VGFX200K/VGFX350K

High Performance FX Series Gate Arrays

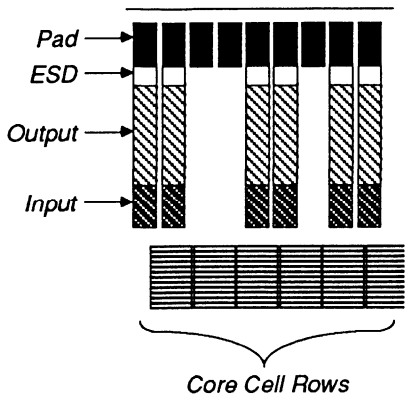
Features

- Superior performance: High speed/low power
- Ultra high density channelless architecture
- Four layer aluminum interconnect
- Proven 0.6 μ H-GaAs E/D MESFET process
- Array performance:
  - D Flip-flop toggle rates: >1.6 GHz
  - Typical gate delay: 115 ps @ 0.15 mW *(Unbuffered 2-input NOR, F.O.=1, 0.21 mm wire)*
  - Typical gate delay: 130 ps @ 0.6 mW *(Buffered 2-input NOR, F.O. = 3, 0.63 mm wire)*
  - ECLGaAs, or TTL compatible inputs/outputs
- Choice of sizes:
  - VGFX100K, 102K 2-Input NOR gates (raw), over 50,000 usable gates or 6,250 usable D flip-flops, 196 I/O
  - VGFX200K, 195K 2-Input NOR gates (raw), over 100,000 usable gates or 12,500 usable D flip flops, 256 I/O
- Multiple buffering options for macrocells
- Embedded SRAM and megacells available
- Supported on MENTOR or VALID platforms
- Behavioral and mixed mode simulation support for VERILOG XL™
- Logic synthesis supported with Synopsys Design Compiler™

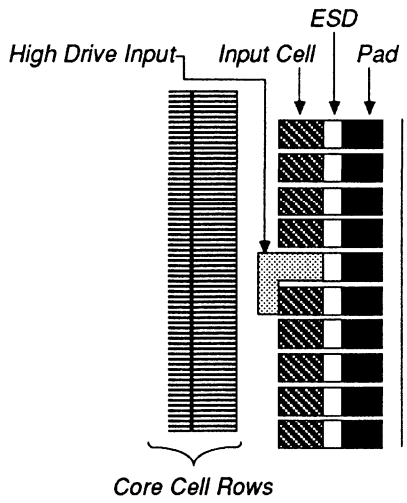
Photomicrograph of the VGFX100K



VGFX100K I/O Cell Detail



VGFX100K Input Cell Detail



Introduction

The FX Series of gate arrays from Vitesse offers the integration level of BiCMOS gate arrays at the speed performance of ECL devices. Implemented using Vitesse's proprietary H-GaAs III process, the VGFX100K, VGFX200K, and VGFX350K are the first in a series of gate arrays that combine ultra high integration with leading edge GaAs performance.

The FX array series utilizes a channelless architecture which allows metal routing on the first layer to be placed directly over unused cells. This approach eliminates pre-defined channels between columns of macros, allowing much greater density and flexibility than channelled architectures. Due to an advanced four layer metal process, typical utilization ranges from 50% to 70%. This yields over 50,000, 100,000, and 175,000 utilizable gates (2-input NOR gates) for the VGFX100K, VGFX200K, and VGFX350K, respectively.

Capable of operating from 50MHz to well over 500 MHz, the FX Series provide the best speed - power performance of any gate array technology currently available.

The speed of leading ECL technology is achieved at a fraction of the power. In addition, power dissipation is lower than similar density BiCMOS arrays at frequencies above 50 to 80 MHz, due to the frequency independent power needs of H-GaAs technology. And with pricing on par with high density BiCMOS, the power savings offered by FX arrays can add up to substantial cost savings to users in terms of overall cooling requirements.

As with all of Vitesse's ASIC products, the FX arrays interface with TTL, ECL, and GaAs devices directly. These arrays use standard power supplies and are supported on the ASIC industry's most popular CAE platforms for schematic capture, behavioral modeling, and logic synthesis. Vitesse also supports the custom implementation of embedded SRAM, multiport register files, and other megacell functions in the FX arrays.

Technology

The FX Series arrays are implemented using Vitesse's proprietary H-GaAs III process. This process represents the third generation of the original H-GaAs technology developed in 1986 by Vitesse to manufacture high yielding, LSI and VLSI digital GaAs circuits. The H-

GaAs III process features a 0.6 μm self-aligned gate MESFET and four levels of metal interconnect. The basic logic structure for the FX Series is a 2-input NOR gate implemented using direct coupled FET logic (DCFL). Millions of hours of life testing have proven the reliability of the H-GaAs process technology and the DCFL logic structure.

Applications

The FX Series of gate arrays are ideal for a wide variety of applications including computers, communications, test, and general instrumentation equipment. This family of high performance semi-custom products is ideally suited for systems requiring very high speed, low power digital logic at high levels of integration.

Computers

The ultra high integration that the FX arrays offer, combined with their high performance and low power consumption, makes them ideally suited for the implementation of high performance processors and processor support logic. Offering a big performance increase over BiCMOS technology and substantially lower power than ECL technology, the FX Series gate arrays are the perfect choice for systems with clock rates in excess of 50 MHz. Specific computer applications for FX arrays include core microprocessors, integer arithmetic processing, floating-point processing, cache control, and bus interface functions.

Communications

Intelligent fiber optic communication links for voice and data transmission can be designed with the FX family. These applications can greatly benefit from the low power dissipation inherent in the FX arrays while allowing the user to implement the high speed VLSI and LSI circuits necessary to handle the new generation of high-bandwidth telecommunications standards. The implementation of large switching networks on a single chip is just one example of these applications.

Architecture

The FX arrays contain four cell types: internal logic cells, input only cells, input/output (I/O) cells, and clock receivers. A photomicrograph of the VGFX100K is shown on page 1-1. Details of I/O and input cells are shown on page 1-2. The table below is a summary of the internal cells, I/O, and package options for the FX Series of gate arrays.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements required for each logic function. The primitive element or building block is a cell which consists of a single depletion-mode transistor and two enhancement-mode transistors which can be connected to make a 2-input NOR gate.

Table 1: *Array Cell Summary*

Array Name	# of Internal Gates		# of Input Cells			# of I/O Cells		Total Signal Pins	Package Options
	Total Raw Cells	2-In* NORs / D F-F*	TTL	ECL GaAs	Hi-Drive	TTL	ECL GaAs		
VGFX100K	102K	51K / 6K	88	88	8	100	100	196	211 pin PGA** 256 pin LDCC
VGFX200K	195K	98K / 12K	92	92	8	156	156	256	344 pin LDCC
VGFX350K(1)	353K	177K / 22K	128	128	—	220	248	376	TBD

(1) Preliminary information only. Please contact a Vitesse Applications Engineer for changes, if any.
** based on 50% utilization*
*** 172 total signal pins supported in this package*

Input Cells

Input only cells are located on two sides of the periphery of the array. Input cells are also located in input/output cells. Input cells can be personalized as latches, flip-flops, or buffers and are compatible with TTL, ECL, or 'native' GaAs signals. All three signal levels can be used in one chip design to optimize overall system performance. In addition, boundary scan can be easily accommodated since each input cell can be configured as a scan flip-flop.Input cells can provide 1x or 2x drive on either the true or complement signal. The input cells translate off-chip logic levels to internal GaAs logic levels. These cells also provide ESD input protection.

Clock Receivers

A number of input cells in each array are configured as high-drive receivers intended for use as clock buffers. These special input cells can support up to 6x the drive capability of a standard input cell.

Input/Output (I/O) Cells

Input/Output cells are located on the top and bottom of the array. I/O cells can be configured as output drivers, input receivers, or bidirectional transceivers. TTL, ECL, and GaAs I/O signal levels are supported with no restrictions on mixing different I/O types. The output portion of the I/O cell can be configured as a latch, flip-flop, 2 or 3-input OR or NOR, or as an inverting or non-inverting buffer. In addition, boundary scan can be easily accommodated since each I/O cell can be configured as a scan flip-flop. When configured as an ECL driver, the output cell can interface with ECL 10KH or 100K receivers while driving a 50Ω load. Two output cells may be paralleled to drive a double-terminated ECL bus (25Ω DC load).

Macro Library

The FX Macro Library contains information to fully evaluate the function and performance of logic blocks (macrocells). The FX library includes functional equivalents for all FURY Series macros as well as optimized megacell functions. The following is a representative list of macrocells which are available for FX arrays. Performance characteristics for selected macros are given on page 4. For a complete set of specifications, refer to the FX Series Gate Array Design Manual.

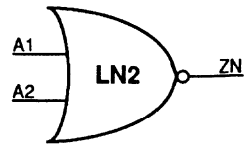
Name	Description	# of Cells
Input/Output Macros		
BIE	Bidirectional ECL Input/Output Buffer	1 I/O Cell
BIE25NR2	Bi-Directional ECL Input/25Ω Output Buffer with 2-input NOR Gate, 2x Drive	2 I/O Cells
BIE25NR3	Bi-Directional ECL Input/25Ω Output Buffer with 3-input NOR Gate, 2x Drive	2 I/O Cells
BIENR2	Bi-Directional ECL Input/25Ω Output Buffer with 2-input NOR Gate, 2x Drive	1 I/O Cell
BIT	Bidirectional TTL Input/Output Buffer	1 I/O Cell
BITOC	Bidirectional TTL Input/Output - Open Drain	1 I/O Cell
IE1F	Inverting ECL Input Buffer, 1x Drive	1 I/O Cell
IE1T	ECL Input Buffer, 1x Drive	1 Input Cell
IE2T	ECL Input Buffer, 2x Drive	1 Input Cell
IECK3	ECL Input Buffer, 3x Drive	1 High Drive Input Cell
IEDIF2	Differential ECL Input, 2x Drive	2 Input Cells
IEDIF3	Differential ECL Input, 3x Drive1High Drive & 1Std Input Cell	
IEDIFF	Differential ECL Input, 1x Drive	2 Input Cells
IG	GaAs Input Buffer, 2x Drive	1 Input Cell
IT1T	TTL Input Buffer	1 Input Cell
LB1UG	GaAs Input Buffer, 1x Drive	6
LB3UG	Inverting GaAs Input Buffer, 1x Drive	6
OE	ECL Output Buffer	1 I/O Cell
OE25	ECL 25Ω Cut-off Output Buffer	2 I/O Cells
OEMDF	ECL Output Buffer With Scan Register, 0.5x Drive	1 I/O Cell
OENOR3	ECL Output Buffer With 3-input NOR	1 I/O Cell
OESD	Differential ECL Output with Single-Ended Input	2 I/O Cells
OG	GaAs Output Buffer	1 I/O Cell
OT	TTL Output Buffer	1 I/O Cell
Buffers		
CLK1	Clock Buffer	8
CLK1G	Clock Buffer with GaAs Input	14
LB3	Dual Inverter, 1x Drive	4
LDR1	Line Driver/Inverting Clock Buffer, 1x Drive	4
LDR3	Line Driver/Inverting Clock Buffer, 3x Drive	12
Flip-Flops		
CNT1	Toggle D Flip-flop	34
LFP1	Positive Edge Triggered D Flip-flop, 2x Drive	12
LFP1B	Positive Edge Triggered D Flip-flop, 3x Drive	14
LFP1U	Positive Edge Triggered D Flip-flop, 1x Drive	10
LFP3	Positive Edge Triggered D Flip-flop with Asynchronous Set & Clear, 2x Drive	16
LFP3U	Positive Edge Triggered D Flip-flop with Asynchronous Set & Clear, 1x Drive	12
LFP4	Positive Edge Triggered D Flip-flop with 3-input OR and Asynchronous Set	18
LFP5	Positive Edge Triggered D Flip-flop with 4-input OR	16

Name	Description	# of Cells
Flip-Flops (cont.)		
LSP1	Positive Edge Triggered D Flip-flop with 2:1 Multiplexer Input, 2x Drive	16
LSP1U	Positive Edge Triggered D Flip-flop with 2:1 Multiplexer Input, 1x Drive	14
Logic Gates		
LA1	Half-adder, 1x Drive	12
LA1U	Half-adder, 2x Drive	6
LA2	Full-adder, 2x Drive	24
LA2B	Full-adder, 3x Drive	32
LA2U	Full-adder, 1x Drive	16
LAND	2-Input AND, 2x Drive	6
LANDU	2-Input AND, 1x Drive	4
LLP1	High Transparent D Latch, 2x Drive	8
LLP1U	High Transparent D Latch, 1x Drive	4
LLP2	High Transparent D Latch with 2-Input OR	8
LLP3	Multiplexed Positive Transparent D Latch	12
LM1	2:1 Multiplexer, 2x Drive	8
LM1U	2:1 Multiplexer, 1x Drive	4
LM3	4:1 Multiplexer, 2x Drive	16
LM3U	4:1 Multiplexer, 1x Drive	12
LN2	2-Input NOR, 2x Drive	4
LN2B	2-Input NOR, 3x Drive	8
LN2U	Dual 2-Input NOR, 1x Drive	4
LN3	3-Input NOR, 1x Drive	6
LN4	4-Input NOR, 2x Drive	8
LN4B	4-Input NOR, 3x Drive	12
LN4U	4-Input NOR, 1x Drive	4
LN9	9-Input NOR, 2x Drive	14
LN9B	9-Input NOR, 3x Drive	18
LN9U	9-Input NOR, 1x Drive	10
LNA2	2-Input NAND, 2x Drive	8
LNA2U	2-Input NAND, 1x Drive	4
LO2	2-Input OR, 1x Drive	6
LO2B	2-Input OR, 2x Drive	8
LO2U	2-Input OR, 0.5x Drive	4
LO4	4-Input OR, 2x Drive	6
LO4B	4-Input OR, 3x Drive	10
LO4U	4-Input OR, 1x Drive	4
LX1	2-Input Exclusive OR, 2x Drive	8
LX1U	2-Input Exclusive OR, 1x Drive	6
LX2	2-Input Exclusive NOR, 2x Drive	8
LX2U	2-Input Exclusive NOR, 1x Drive	4
Miscellaneous		
PD	Pull Down	1

Selected Macrocell AC Performance (Commercial temp. arrays)

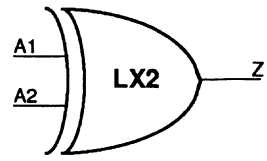
LN2: Buffered 2-Input NOR

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
A1, A2 to ZN	*Rising Signal*	50	—	80	ps
	Falling Signal	40	—	50	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	8	ps
	Falling Signal	7	—	8	ps
Delay/mm wire	*Rising Signal*	92	—	150	ps
	Falling Signal	76	—	95	ps
Power Dissipation		—	0.50	0.79	mW



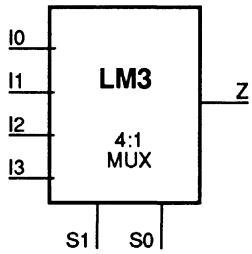
LX2: 2-Input XNOR

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
A1, A2 to Z	*Rising Signal*	120	—	320	ps
	Falling Signal	150	—	290	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	8	ps
	Falling Signal	9	—	11	ps
Delay/mm wire	*Rising Signal*	92	—	150	ps
	Falling Signal	97	—	121	ps
Power Dissipation		—	0.99	1.53	mW



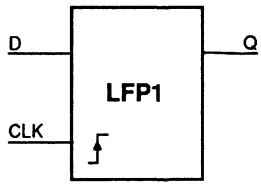
LM3: 4:1 Multiplexer

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
S0, S1 to Z	*Rising Signal*	170	—	350	ps
	Falling Signal	170	—	320	ps
I0 - I3 to Z	*Rising Signal*	170	—	210	ps
	Falling Signal	170	—	260	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	6	—	9	ps
	Falling Signal	9	—	11	ps
Delay/mm wire	*Rising Signal*	103	—	167	ps
	Falling Signal	97	—	121	ps
Power Dissipation		—	1.40	2.28	mW



LFP1: Positive Edge Triggered D Flip-flop

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
CLK to Q	*Rising Signal*	110	—	180	ps
	Falling Signal	240	—	300	ps
t_{SET-UP}		61	—	102	ps
t_{HOLD}		43	—	73	ps
Toggle freq. (based on min. pulse width)		1620	—	2710	MHz
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	5	—	8	ps
	Falling Signal	8	—	10	ps
Delay/mm wire	*Rising Signal*	92	—	150	ps
	Falling Signal	92	—	115	ps
Power Dissipation		—	1.76	2.77	mW



Absolute Maximum Ratings (1)

Power Supply Voltage (ECL), V_{TT} potential to GND ..... -2.5V to +0.5V
Power Supply Voltage (TTL), V_{TTL} potential to GND ..... +4.0V to -0.5V
Power Supply Voltage (TTL), V_{TTL}, potential to GND *(VGFX350K)* ..... +4.0V to -0.5V (if core at 0, -2.0 V)
..... +6.0V to -0.5V (if core at 2.0, 0 V)
ECL Input Voltage Applied, $(V_{IN\ ECL})$ ..... +0.5V to V_{TT}
TTL Input Voltage Applied, $(V_{IN\ TTL})$ ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HI) ..... 50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65°C to +150°C

Recommended Operating Conditions

ECL Supply Voltage, (V_{TT}) ..... -2.0V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +3.3V ± 5%
TTL Supply Voltage, (V_{TTL}) *(VGFX350K)* ..... +3.3V ± 5% (if core at 0, -2.0 V)
..... +5.0V to ± 5% (if core at 2.0, 0 V)
Commercial Operating Temperature Range, (T) (2). ..... 0° to 70°C
Industrial Operating Temperature Range, (T) (2). ..... -40° to 85°C

Notes:
(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit is ambient temperature and upper limit is case temperature.

DC Characteristics

TTL Inputs/Outputs: *(Over recommended commercial operating conditions, TTLGND = GND)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	V_{TTL}	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	V_{CC}	—	0.5	V	I_{OL} = 16 mA
V_{IH}	Input HIGH voltage	2.0	—	V_{TTL} ± 1.0 V	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	—	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

ECL Inputs/Outputs:

(Over recommended operating conditions with internal V_{REF}. $V_{CC} = V_{CCA}$ = GND, Output load 50Ω to V_{TT})

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	Guaranteed HIGH for all inputs
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed LOW for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	$V_{IN} = V_{IH}$ max
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IL}$ min
I_{IL}	Input LOW current	-50	—	—	µA	

Note: 1) Differential ECL output pins must be terminated identically.

GaAs Inputs/Outputs:

(Over recommended commercial operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load 50Ω to V_{TT})

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	V_{TT}+700	—	V_{TT}+1400	mV	
V_{OL}	Output LOW voltage	V_{TT}	—	V_{TT}+100	mV	
V_{IH}	Input HIGH voltage	V_{TT}+600	—	V_{TT}+1200	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TT}-400	—	V_{TT}+200	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-100	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential GaAs output pins must be terminated identically.
2) If only GaAs I/Os are used, V_{TT} = 0V, V_{CC} = +2.0V, and all I/O levels are still referenced to V_{TT}.

Option Development Procedure

Vitesse Semiconductor offers customers the option of designing their own gate array or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse implementation en-gineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are always performed by a Vitesse implementation engineer.

- Final placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Design rule checking and layout vs schematic

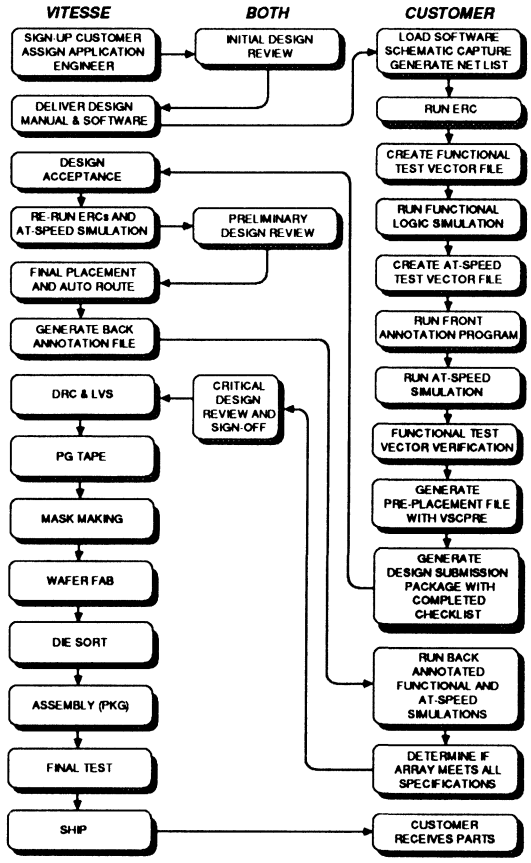
Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart at right summarizes the typical gate array project flow and the various tasks delegated to the customer and/or Vitesse.

CAD Tools/Support

FX designs are supported on MENTOR, VALID, SYNOPSYS, and VERILOG platforms. LASAR simulation software is used to verify the AC performance of the design by taking into account on-chip timing variations. Simulation libraries for VERILOG XL™ are also supported.

The Vitesse Design Kit includes documentation and software which allow the customer to per-form schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation upon completion of placement and routing. To facilitate floorplanning and block pre-placement, Vitesse has an interactive graphical placement program that the customer may choose to use for their design. This program is supported in the X Windows™ environment. Cadence placement and routing tools are used for physical implementation.

Gate Array Design Flow



Training

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

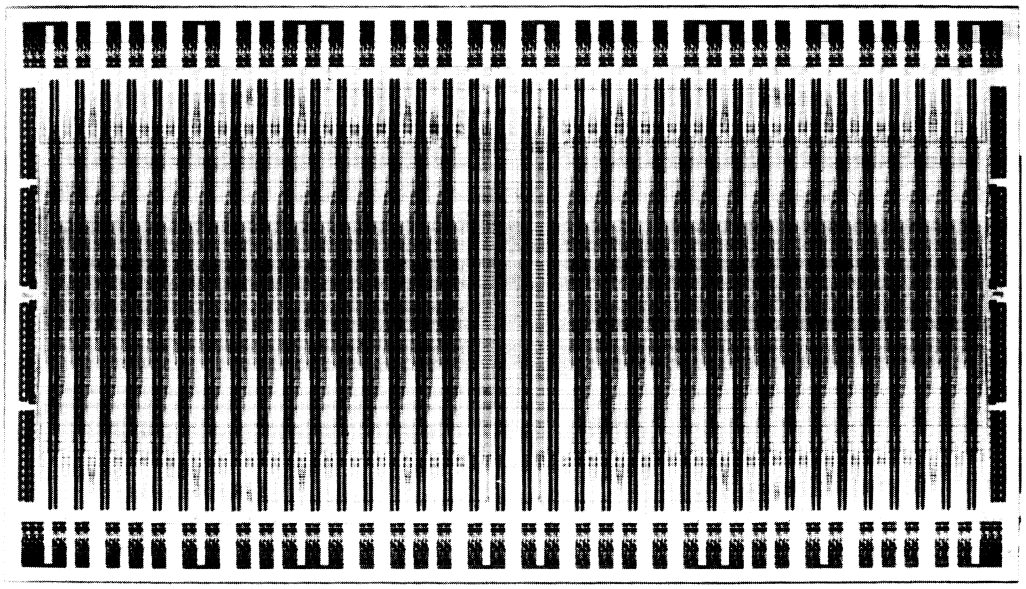
VSC3K/VSC5K/VSC10K/VSC15K/VSC20K8R/VSC30K

High Performance FURY Series Gate Arrays

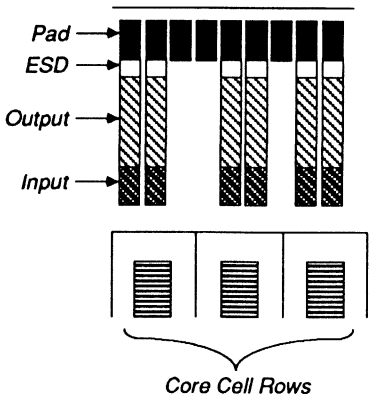
Features

- Superior performance: High speed/low power
- High density channelled architecture (up to 100% utilization)
- Proven 0.8µ H-GaAs E/D MESFET process
- Array performance
  - D flip-flop toggle rates: >1 GHz
  - Typical gate delay: 177 ps @ 1.1 mW *(2-input NOR, F.O. = 3, 1.5 mm wire)*
  - ECL and GaAs inputs/outputs at 1 GHz
  - TTL inputs/outputs at 100 MHz
  - Typical speed-power product: ~0.025 pJ *(2-input NOR)*
- SRAM performance
  - Cycle time: 3.5 ns (min)
  - Clock to Q: 1.5 ns (max)
  - Power dissipation: 0.55 W (Typical per 1K cell)
  - Normal and scan mode
  - Dedicated test circuitry
- ECL, GaAs, or TTL compatible inputs/outputs
- Choice of sizes: from VSC3K *(3,584 2-Input NOR gates)*, to VSC30K *(30,528 2-Input NOR gates)*
- Choice of buffered or unbuffered gates
- Three temperature ranges
  - Commercial: 0° to +70° C
  - Industrial: -40° to +85° C
  - Military: -55° to +125° C
- Multiple buffering options for macrocells
- Embedded SRAM and megacells available
- Mil-Std-883C, Level B screening and qualification available
- Supported on MENTOR, DAISY or VALID platforms
- Behavioral and mixed mode simulation support for VERILOG XL
- Logic synthesis supported with Synopsis Design Compiler™

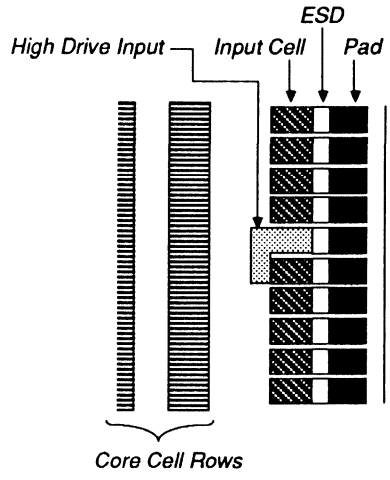
Photomicrograph of the VSC30K



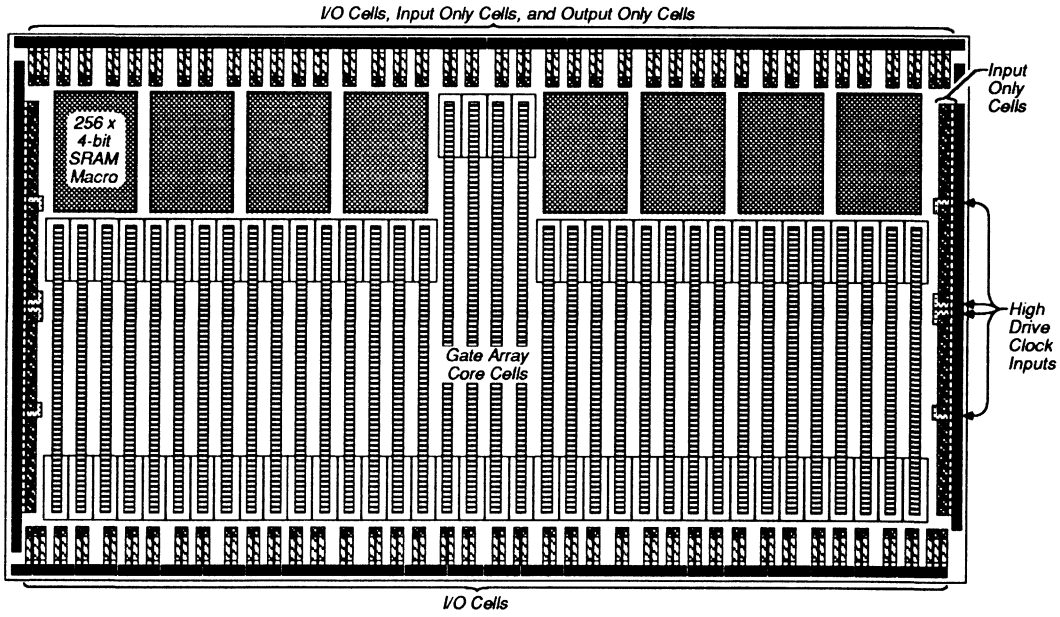
FURY I/O Cell Detail



FURY Input Cell Detail



Architecture - The VSC20K8R



Introduction

The VSC3K, VSC5K, VSC10K, VSC15K, VSC20K8R, and VSC30K are members of the FURY Series of high performance gate arrays. They are ideally suited for systems which require high density, state-of-the-art performance while maintaining low power dissipation. Vitesse uses a proprietary high yielding 0.8μ GaAs MESFET process to build the FURY Series gate arrays. These arrays interface with TTL, ECL and GaAs technologies without adding any additional system requirements. The FURY family offers speed performance equal to or better than leading edge ECL gate arrays, while dissipating only 1/3 to 1/4 of the power. This can add up to substantial cost savings to users in terms of overall cooling requirements.

The interface architecture of the FURY series allows the user to take advantage of GaAs I/O levels, allowing ultra-high speed, low power communication between other GaAs devices in the system.

Input cells and output cells can be configured to contain a positive edge triggered D flip-flop and can support boundary scan designs. The combination of internal logic and I/O cells in the FURY Series provide the user with complexities ranging from 3500 to over 30,000 equivalent gates.

Applications

The FURY Series of gate arrays can be used in a wide variety of applications including: computers, communications, test, and general instrumentation. This family of high performance semi-custom products is ideally suited for systems requiring very high speed, low power digital logic at high levels of integration.

Computers

Existing mainframe systems utilizing ECL or TTL technologies can improve speed and reduce power dissipation with the FURY arrays. Super-minis using ECL arrays can increase system performance while reducing overall cooling requirements. Workstations using standard microprocessors can bring supercomputing power to their system by using the FURY arrays.

Communications

Fiber optic communication links for voice and data transmission can be designed with the FURY family. These applications can greatly benefit from the low power dissipation inherent in the FURY arrays while allowing the user to implement the high speed VLSI and LSI circuits necessary to handle the new generation of telecommunications standards.

Array Name	# of Internal Gates		# of Input Cells		# of I/O Cells	Output Only Cells	Total Signal Pins	Package Options
	Total Cells	2-in NORs / D F-F	TTL, ECL, GaAs	Hi-Drive	TTL, ECL, GaAs			
VSC3K	3,584	3,584 / 290	40	4	52	—	92	132 pin LDCC
VSC5K	6,400	6,400 / 520	52	4	68	—	120	149 pin PGA 164 pin LDCC
VSC10K	13,376	13,376 / 1,100	74	8	100	—	174	211 pin PGA
			96	8	100	—	196	256 pin LDCC
VSC15K	16,896	16,896 / 1,408	74	8	100	—	174	211 pin PGA
			96	8	100	—	196	256 pin LDCC
VSC20K8R	20,736	20,736 / 1,728	96	8	132	19	256	344 pin LDCC
VSC30K	30,528	30,528 / 2,544	100	8	156	—	256	344 pin LDCC

Architecture

The FURY arrays all contain four basic cell types: internal logic cells, input only cells, input/output (I/O) cells, and clock receivers. The VSC20K8R contains two additional cell types: the output only cell and the 256 x 4 bit SRAM macrocell. A photomicrograph of the VSC30K is shown on page 1-10, and the architecture of the VSC20K8R is shown on page 1-11. The table below is a summary of the internal cells, I/O, and package options for the FURY Series of gate arrays.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion transistor and two enhancement transistors which can be connected to make a 2-input NOR gate.

Input Cells

Input only cells are located on two sides of the periphery of the array. Input cells are also located in input/output cells. Input cells can be personalized as latches, flip-flops, or buffers and are compatible with TTL, ECL, or 'native' GaAs signals. All three signal levels can be used in one chip design to optimize overall system performance. Input cells can provide 1x or 2x drive on either the true or complement signal. The input cells translate off-chip logic levels to internal GaAs logic levels. These cells also provide ESD input protection.

Clock Receivers

A number of input cells in each array are configured as high-drive receivers intended for use as clock buffers. These special input cells can support up to 6x the drive capability of a standard input cell.

Input/Output (I/O) Cells

Input/output cells are located on two sides of the periphery of the array. I/O cells contain both input and output cells and can be configured as outputs, bidirectionals or inputs. I/O cells are compatible with TTL, ECL or 'native' GaAs signals.

Output Cells

Output cells are only located in I/O cells. These cells can be configured as latches, flip-flops, 2- or 3-input ORs or NORs, or as inverting or non-inverting output buffers compatible with TTL, ECL or 'native' GaAs signal levels. The output cells are capable of providing ECL 10K, 10KH, or 100K levels across external 50Ω loads to V_{TT}. Two output drivers can be connected in parallel to provide 25Ω drive.

SRAM Cells *(VSC20K8R only)*

8K bits of SRAM cells are embedded in the VSC20K8R for combined logic and RAM applications. The SRAM is organized into 8 blocks 256x4. The SRAM support dedicated circuitry and a scan mode.

Output Only Cells *(VSC20K8R only)*

Output Only cells are located along the top of the array. These cells can be configured as latches, flip-flops, 2- or 3-input ORs or NORs, or as inverting or non-inverting output buffers compatible with TTL, ECL or 'native' GaAs signal levels. The output cells are capable of providing ECL 10K, or 100K levels across external 50Ω loads to V_{TT}. Two output drivers can be connected in parallel to provide 25Ω drive.

Macro Library

The FURY Macro Library contains information to fully evaluate the function and performance of logic blocks (macrocells). These macrocells define the optimized interconnection pattern of transistors in one or more cells which have been utilized to perform a logic function. The following page contains a representative list of macrocells which are available for FURY arrays. Performance characteristics for selected macros are given on page 1-15. For complete specifications, refer to the FURY Series Gate Array Design Manual.

Name	Description	# of Cells
Input/Output Macros		
BIE	Bidirectional ECL Input/Output Buffer	1 I/O Cell
BIE25NR2	Bi-Directional ECL Input/25Ω Output Buffer with 2-input NOR Gate, 2x Drive	2 I/O Cells
BIE25NR3	Bi-Directional ECL Input/25Ω Output Buffer with 3-input NOR Gate, 2x Drive	2 I/O Cells
BIENR2	Bi-Directional ECL Input/25Ω Output Buffer with 2-input NOR Gate, 2x Drive	1 I/O Cell
BIT	Bidirectional TTL Input/Output Buffer	1 I/O Cell
BITOC	Bidirectional TTL Input/Output - Open Drain	1 I/O Cell
IE1F	Inverting ECL Input Buffer, 1x Drive	1 I/O Cell
IE1T	ECL Input Buffer, 1x Drive	1 Input Cell
IE2T	ECL Input Buffer, 2x Drive	1 Input Cell
IECK3	ECL Input Buffer, 3x Drive	1 High Drive Input Cell
IEDIF2	Differential ECL Input, 2x Drive	2 Input Cells
IEDIF3	Differential ECL Input, 3x Drive1High Drive & 1Std Input Cell	
IEDIFF	Differential ECL Input, 1x Drive	2 Input Cells
IG	GaAs Input Buffer, 2x Drive	1 Input Cell
IT1T	TTL Input Buffer	1 Input Cell
LB1UG	GaAs Input Buffer, 1x Drive	2
LB3UG	Inverting GaAs Input Buffer, 1x Drive	2
OE	ECL Output Buffer	1 I/O Cell
OE25	ECL 25Ω Cut-off Output Buffer	2 I/O Cells
OEMDF	ECL Output Buffer With Scan Register, 0.5x Drive	1 I/O Cell
OENOR3	ECL Output Buffer With 3-input NOR	1 I/O Cell
OESD	Differential ECL Output with Single-Ended Input	2 I/O Cells
OG	GaAs Output Buffer	1 I/O Cell
OT	TTL Output Buffer	1 I/O Cell
Buffers		
CLK1	Clock Buffer	8
CLK1G	Clock Buffer with GaAs Input	8
LB3	Dual Inverter, 1x Drive	2
LDR1	Line Driver/Inverting Clock Buffer, 1x Drive	4
LDR3	Line Driver/Inverting Clock Buffer, 3x Drive	12
Flip-Flops		
CNT1	Toggle D Flip-flop	34
LFP1	Positive Edge Triggered D Flip-flop, 2x Drive	12
LFP1B	Positive Edge Triggered D Flip-flop, 3x Drive	14
LFP1U	Positive Edge Triggered D Flip-flop, 1x Drive	10
LFP3	Positive Edge Triggered D Flip-flop with Asynchronous Set & Clear, 2x Drive	14
LFP3U	Positive Edge Triggered D Flip-flop with Asynchronous Set & Clear, 1x Drive	10
LFP4	Positive Edge Triggered D Flip-flop with 3-Input OR and Asynchronous Set	14
LFP5	Positive Edge Triggered D Flip-flop with 4-Input OR	14

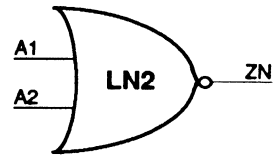
Name	Description	# of Cells
Flip-Flops (cont.)		
LSP1	Positive Edge Triggered D Flip-flop with 2:1 Multiplexer Input, 2x Drive	16
LSP1U	Positive Edge Triggered D Flip-flop with 2:1 Multiplexer Input, 1x Drive	12
Logic Gates		
LA1	Half-adder, 1x Drive	12
LA1U	Half-adder, 2x Drive	6
LA2	Full-adder, 2x Drive	22
LA2B	Full-adder, 3x Drive	28
LA2U	Full-adder, 1x Drive	14
LAND	2-Input AND, 2x Drive	6
LANDU	2-Input AND, 1x Drive	4
LLP1	High Transparent D Latch, 2x Drive	8
LLP1U	High Transparent D Latch, 1x Drive	4
LLP2	High Transparent D Latch with 2-Input OR	8
LLP3	Multiplexed Positive Transparent D Latch	12
LM1	2:1 Multiplexer, 2x Drive	8
LM1U	2:1 Multiplexer, 1x Drive	4
LM3	4:1 Multiplexer, 2x Drive	14
LM3U	4:1 Multiplexer, 1x Drive	10
LN2	2-Input NOR, 2x Drive	4
LN2B	2-Input NOR, 3x Drive	8
LN2U	Dual 2-Input NOR, 1x Drive	2
LN3	3-Input NOR, 1x Drive	6
LN4	4-Input NOR, 2x Drive	8
LN4B	4-Input NOR, 3x Drive	12
LN4U	4-Input NOR, 1x Drive	2
LN9	9-Input NOR, 2x Drive	12
LN9B	9-Input NOR, 3x Drive	14
LN9U	9-Input NOR, 1x Drive	8
LNA2	2-Input NAND, 2x Drive	8
LNA2U	2-Input NAND, 1x Drive	4
LO2	2-Input OR, 1x Drive	6
LO2B	2-Input OR, 2x Drive	8
LO2U	2-Input OR, 0.5x Drive	2
LO4	4-Input OR, 2x Drive	6
LO4B	4-Input OR, 3x Drive	8
LO4U	4-Input OR, 1x Drive	4
LX1	2-Input Exclusive OR, 2x Drive	8
LX1U	2-Input Exclusive OR, 1x Drive	6
LX2	2-Input Exclusive NOR. 2x Drive	8
LX2U	2-Input Exclusive NOR, 1x Drive	4
R256X4	256 x 4 Bit SRAM	4
Miscellaneous		
PD	Pull Down	2

Selected Macrocell AC Performance (Commercial arrays)

(V_{TT} = -2.0V, V_{TTL} = +5.0V, V_{CC} = V_{CCA} = GND, T_C = 25° C, Load: F.O. = Ø; Ø mm wire.)

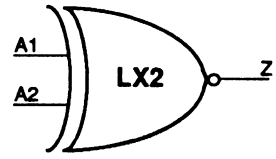
LN2: Buffered 2-input NOR

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to ZN	*Rising Signal*	68	—	111	ps
	Falling Signal	58	—	73	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	8	—	10	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	31	—	39	ps
Power Dissipation		—	1.1	1.8	mW



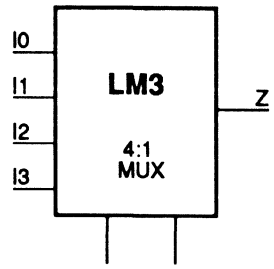
LX2: 2-input XNOR

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to Z	*Rising Signal*	279	—	455	ps
	Falling Signal	349	—	437	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	11	—	13	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	40	—	50	ps
Power Dissipation		—	2.2	3.4	mW



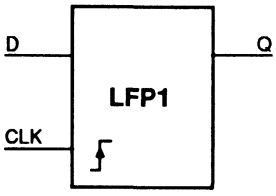
LM3: 4:1 Multiplexer

Parameter		Min	Typ	Max	Units
Propagation Delay					
S0, S1 to Z	*Rising Signal*	298	—	485	ps
	Falling Signal	382	—	478	ps
I0 - I3 to Z	*Rising Signal*	174	—	283	ps
	Falling Signal	307	—	385	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	10	—	16	ps
	Falling Signal	11	—	13	ps
Delay/mm wire	*Rising Signal*	59	—	97	ps
	Falling Signal	40	—	50	ps
Power Dissipation		—	3.1	5.1	mW



LFP1: Positive Edge Triggered D Flip-flop

Parameter		Min	Typ	Max	Units
Propagation Delay					
CLK to Q	*Rising Signal*	155	—	253	ps
	Falling Signal	349	—	437	ps
t_{SET-UP}		—	—	146	ps
t_{HOLD}		—	—	104	ps
Toggle frequency		874	—	—	MHz
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	10	—	13	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	38	—	47	ps
Power Dissipation		—	3.9	6.2	mW



DC Characteristics

TTL Inputs/Outputs: *(Over recommended operating conditions, TTLGND = GND)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	V_{TTL}	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	V_{CC}	—	0.5	V	I_{OL} = 16 mA
V_{IH}	Input HIGH voltage	2.0	—	—	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	—	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

ECL Inputs/Outputs: *(Over recommended operating conditions with internal V_{REF}. $V_{CC} = V_{CCA}$ = GND, Output load 50Ω to V_{TT})*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential ECL output pins must be terminated identically.

GaAs Inputs/Outputs: *(Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load 50Ω to V_{TT})*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	V_{TT}+700	—	V_{TT}+1400	mV	
V_{OL}	Output LOW voltage	V_{TT}	—	V_{TT}+100	mV	
V_{IH}	Input HIGH voltage	V_{TT}+600	—	V_{TT}+1200	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TT}-400	—	V_{TT}+200	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-100	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential GaAs output pins must be terminated identically.
2) If only GaAs I/Os are used, V_{TT} = 0V, V_{CC} = +2.0V, and all I/O levels are still referenced to V_{TT}.

Absolute Maximum Ratings (1)

Power Supply Voltage (ECL), (V_{TT}) ..... -2.5V to +0.5V
Power Supply Voltage (TTL) (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... +0.5V to V_{TT}
TTL Input Voltage Applied (2), (V_{TTLIN}) ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HI) ..... 50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

2) V_{TT}, V_{TTL} must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.

Recommended Operating Conditions

ECL Power Supply Voltage (1), (V_{TT}) ..... -2.1V to -1.9V
TTL Power Supply Voltage, (V_{TTL}) ..... +4.75V to +5.25V
Operating Temperature (2), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTE: 1) When using internal ECL 100K reference level.

2) Lower limit of specification is ambient temperature and upper limit is case temperature.

Option Development Procedure

Vitesse Semiconductor offers customers the option of designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse application engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are always performed by a Vitesse application engineer.

- Final placement and routing of the design
- Net-length extraction
- Fan-out and metal delay calculation
- Design rule checking and layout vs schematic

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart on page 1-18 summarizes the typical gate array project flow and the various tasks delegated to the customer and/or Vitesse.

CAD Tools/Support

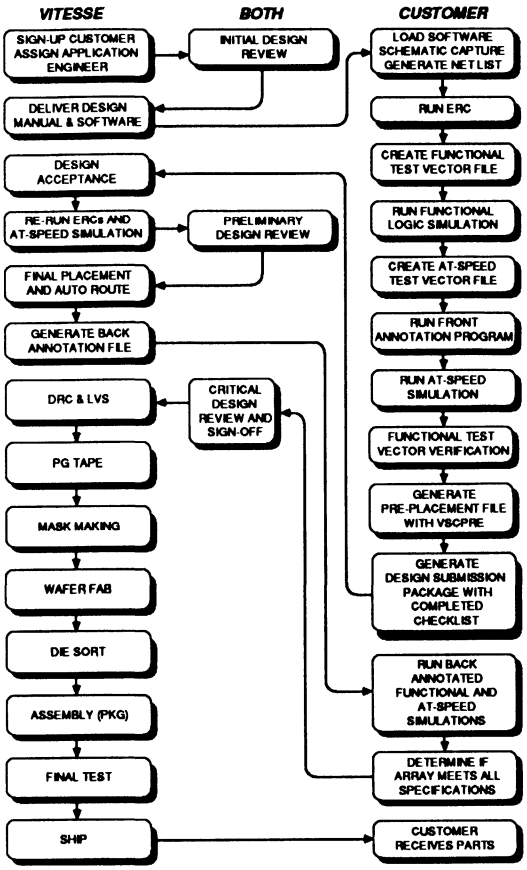
FURY designs are supported on MENTOR, DAISY, and VALID platforms. The logic sysnthesis tool SYNOPSIS is also supported, which will provide a speed optimized gate implementation for behavioral level circuit descriptions to the VERILOG logic simulator.

The Vitesse Design Kit includes documentation and software which allow the customer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation upon completion of placement and routing. Also, Vitesse has an interactive pre-placement program that the customer may choose to use for their design.

Training

Design classes are provided to help the customer understand the design methodology and tools utilized in the gate array design process. These classes are recommended for all customers planning to implement a design in a Vitesse gate array. Training can be provided at the Vitesse facility or at the customer's site.

Gate Array Design Flow



PLR2KT

High Performance - 2400 Gate TTL Compatible GaAs Gate Array

Features

- Superior performance: high speed/low power
- Array performance
  - D flip-flop toggle rates: >1 GHz
  - Typical gate delay: 177 ps @ 1.1 mW *(2-Input NOR, F.O. = 3, 1.5 mm wire)*
  - TTL/CMOS inputs/outputs to support up to 150 MHz state machine design
  - Typical speed-power product: ~0.025 pJ
- 2400 2-input NOR internal gates, 92 signal I/O (Up to 52 outputs or 92 inputs)
- Choice of buffered or unbuffered gates
- Supported on MENTOR, DAISY, or VALID (SUN 3) CAD platforms
- Direct PLD source file conversion using the SYNOPSYS Design Compiler™
- VERILOG-XL™ behavioral modeling and simulation
- Compatible with +5 V only TTL systems (see application note on page 1-26)
- Typical power dissipation: 1.5 W
- Low Cost 132-pin Metal Quad flatpack (MQUAD)

Introduction

TTL signal interface, low power, and 150 MHz performance at very low cost makes the PLR2KT the perfect replacement for multiple programmable logic devices (PLDs) in high speed workstations and PCs. A proprietary high yielding, low power, 0.8μ GaAs MESFET process is used to build the PLR2KT gate array. This product has 2400 usable gates and the I/Os are TTL and CMOS compatible. The PLR2KT can replace 6 to 10 or more PLDs, depending on the application, and offers better performance than today's fastest TTL devices. The resulting reduction in part count can lead to a dramatic savings in power dissipation. The PLR2KT is the ideal replacement for TTL programmable logic devices.

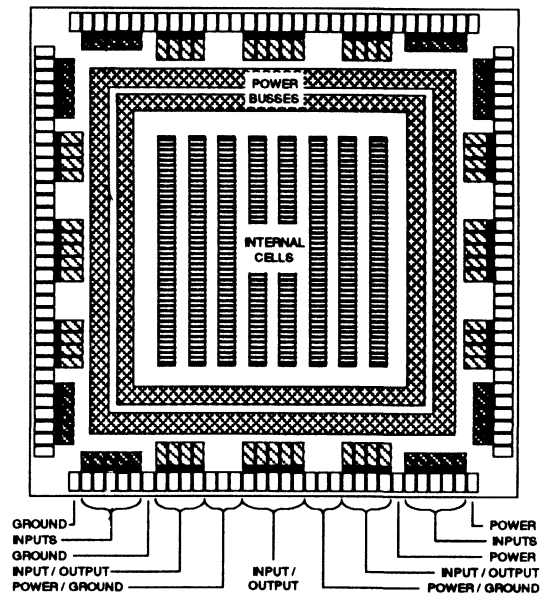
Applications

This array is designed to replace high speed TTL programmable logic devices or glue logic in a wide variety of applications in computers, workstations, communications and instrumentation. With 2400 usable gates, the PLR2KT offers outstanding utility for high performance TTL systems including such functions as peripheral control, communications, and data processing.

The PLR2KT is the ideal interface chip for high speed systems using state-of-the-art 32-bit RISC or CISC microprocessor architectures.

Because of its outstanding flip-flop performance, fast state machines and counters can easily be realized in the PLR2KT. Also, functions such as cache memory control and bus arbitration can be implemented with minimum delay in this highly integrated, low cost solution. Application note 9 (see Section 7, "Application Notes") from Vitesse describes a 50MHz cache controller design using the PLR2KT array.

Architecture



Architecture

The PLR2KT array contains three cell types: internal logic cells, input only cells and input/output cells. The layout of the PLR2KT is shown on page 1-19.

Internal Logic Cells

The internal logic cells comprise most of the area of the array. These cells use direct coupled FET logic (DCFL), which minimizes the number of elements needed for each logic function. The primitive element or building block is a cell which consists of a single depletion transistor and two enhancement transistors which can be connected to make a 2-input NOR gate.

Input-Only Cells

Input-only cells are located on all four sides of the periphery of the array. Input-only cells can be configured to switch at either TTL or CMOS thresholds. All input cells contain ESD input protection.

Input/Output (I/O) Cells

Input/output cells are also located on all four sides of the periphery of the array. Each I/O cell contains a replica of an input-only cell as well as an output cell. Input/output cells can be configured as outputs, bidirectionals or inputs. Outputs are TTL compatible only.

Macro Library

The PLR2KT Macro Library contains information to fully evaluate the function and performance of logic blocks (macrocells) available for the PLR2KT. The PLR2KT macros are identical in function and performance to those in the FURY Military Macrocell Library. These macrocells define the optimized interconnection pattern of transistors in one or more cells which have been utilized to perform a logic function. The following is a representative list of the internal macrocells which are available for the PLR2KT gate array. Performance characteristics for selected macros are given in this data sheet. For a complete set of macro specifications, refer to the PLR2KT Design Manual.

- CLK1 - Clock buffer
- CNT1 - Toggle D flip-flop
- LA1 - Half adder
- LA1U - Half adder, unbuffered
- LA2 - Full adder
- LA2B - Full adder with 2x buffer
- LA2U - Full adder, unbuffered
- LAND - 2-input AND
- LANDU - 2-input AND, unbuffered
- LB3 - Dual inverter, unbuffered
- LDR1 - Line driver/Inverting clock buffer, 1x drive
- LDR3 - Line driver/Inverting clock buffer, 3x drive
- LFP1 - Positive edge triggered D flip-flop
- LFP1B - Positive edge triggered D flip-flop with 2x buffer
- LFP1U - Positive edge triggered D flip-flop, unbuffered
- LFP3 - Positive edge triggered D flip-flop with asynchronous set & clear
- LFP3U - Positive edge triggered D flip-flop with asynchronous set & clear, unbuffered
- LFP4 - Positive edge triggered D flip-flop with 3-input OR and asynchronous set
- LFP5 - Positive edge triggered D flip-flop with 4-input OR
- LLP1 - Positive transparent D latch
- LLP1U - Positive transparent D latch, unbuffered
- LLP2 - Positive transparent D latch with 2-input OR
- LLP3 - Muxed positive transparent D latch
- LM1 - 2:1 multiplexer
- LM1U - 2:1 multiplexer, unbuffered
- LM3 - 4:1 multiplexer
- LM3U - 4:1 multiplexer, unbuffered
- LN2 - 2-input NOR
- LN2B - 2-input NOR with 2x buffer
- LN2U - Dual 2-input NOR, unbuffered
- LN4 - 4-input NOR
- LN4U - 4-input NOR, unbuffered
- LN9 - 9-input NOR
- LN9B - 9-input NOR with 2x buffer
- LN9U - 9-input NOR, unbuffered
- LNA2 - 2-input NAND
- LNA2U - 2-input NAND, unbuffered
- LO2 - 2-input OR
- LO4 - 4-input OR
- LO4B - 4-input OR with 2x buffer
- LO4U - 4-input OR, unbuffered
- LSP1 - Positive edge triggered D flip-flop with 2:1 mux input
- LSP1U - Positive edge triggered D flip-flop with 2:1 mux input, unbuffered
- LX1 - 2-input exclusive OR
- LX1U - 2-input exclusive OR, unbuffered
- LX2 - 2-input exclusive NOR
- LX2U - 2-input exclusive NOR, unbuffered

Absolute Maximum Ratings (1)

Core Logic Supply Voltage, (V_{MM}) ..... +3.0 V to -0.5 V
TTL/CMOS Supply Voltage, (V_{TTL}) ..... +6.0 V to -0.5 V
TTL/CMOS Input Voltage Applied, ($V_{IN\ TTL}$) ..... -0.5 V to V_{TTL}
TTL Output Current, I_{OUT}, (DC, output HI) ..... 50 mA
Maximum Junction Temperature Under Bias, (T_J) ..... 130° C
Storage Temperature, (T_{STG}) ..... -65° C to +150° C

Recommended Operating Conditions

Core Logic Supply Voltage, (V_{MM}) ..... +2.0 V ± 5%
TTL Supply Voltage, (V_{TTL}) ..... +5.0 V ± 5%
Operating Temperature Range, (T) (2). ..... 0° to 70° C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC Characteristics

TTL Inputs/Outputs: *(Over recommended operating conditions)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	—	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	—	—	0.5	V	I_{OL} = 8.0 mA
V_{IH}	Input HIGH voltage	2.0	—	—	V	Guaranteed HIGH for TTL inputs
V_{IL}	Input LOW voltage—	—	0.8	V		Guaranteed LOW for TTL inputs
I_{IH}	Input HIGH current—	—	200	µA		V_{IH} = 2.4 V
I_{IL}	Input LOW current-500	—	—	µA		V_{IL} = 0.0 V
I_{OZH}	3-state output OFF current HIGH	—	—	200	µA	V_{IN} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-200	—	—	µA	V_{IN} = 0.4 V

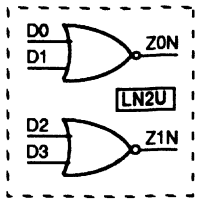
CMOS Inputs: *(Over recommended operating conditions)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	3.5	—	—	V	Guaranteed HIGH for CMOS inputs
V_{IL}	Input LOW voltage	—	—	1.5	V	Guaranteed LOW for CMOS inputs
I_{IH}	Input HIGH current	—	—	200	µA	V_{IH} = V_{TTL} - 1.0 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IL} = 0.0 V

Selected Macrocell AC Performance[1]: *(Over Recommended Operating Conditions)*

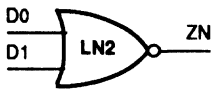
LN2: Unbuffered, Dual 2-input NOR (2 Cells)

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
(D0 - D1 to ZN0,	*Rising Signal*	56	—	91	ps
D2 - D3 to ZN1)	*Falling Signal*	58	—	73	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	54	—	88	ps
	Falling Signal	13	—	15	ps
Delay/mm wire	*Rising Signal*	333	—	543	ps
	Falling Signal	48	—	60	ps
Power Dissipation		0.55	0.63	1.0	mW



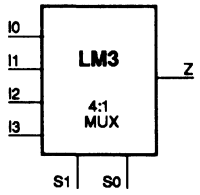
LN2: Buffered 2-input NOR (4 Cells)

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
D0, D1 to ZN	*Rising Signal*	87	—	141	ps
	Falling Signal	66	—	83	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	6	—	7	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	22	—	27	ps
Power Dissipation		1.0	1.1	1.6	mW



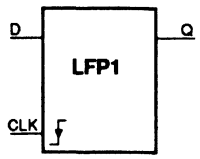
LM3: 4:1 Multiplexer (14 Cells)

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
S0, S1 to Z	*Rising Signal*	280	—	586	ps
	Falling Signal	290	—	570	ps
I0 - I3 to Z	*Rising Signal*	280	—	380	ps
	Falling Signal	290	—	460	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	10	—	16	ps
	Falling Signal	7	—	9	ps
Delay/mm wire	*Rising Signal*	59	—	96	ps
	Falling Signal	28	—	34	ps
Power Dissipation		2.8	3.1	4.6	mW



LFP1: Positive Edge Triggered D Flip-flop (12 Cells)

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
CLK to Q	*Rising Signal*	192	—	313	ps
	Falling Signal	407	—	510	ps
t_{SET-UP}		—	—	187	ps
t_{HOLD}		—	—	135	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	9	—	14	ps
	Falling Signal	7	—	9	ps
Delay/mm wire	*Rising Signal*	53	—	87	ps
	Falling Signal	25	—	32	ps
Power Dissipation		3.4	3.9	5.6	mW

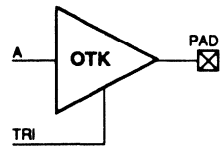


Note: 1) Macrocell AC performance is for user reference and is not explicitly measured.

TTL Output AC Performance [1]: *(Over Recommended Operating Conditions)*

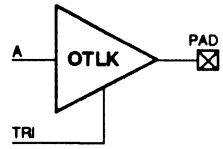
OTK: TTL Output Buffer

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
A to PAD[2]	*Rising Signal*	3290	—	5360	ps
	Falling Signal	4240	—	5310	ps
TRI to PAD (all cases)	*Rising Signal*	3720	—	6060	ps
	Falling Signal	4980	—	6240	ps
Load Dependent Delay					
A to PAD	*Rising Signal*	31	—	51	ps/pF
	Falling Signal	54	—	68	ps/pF
Edge Rates[2], [3]	*Rising Signal*	—	—	2	V/ns
	Falling Signal	—	—	2	V/ns
Peak Current	*Rising Signal*	—	—	55	mA
	Falling Signal	—	—	65	mA
Power Dissipation[4]		—	—	30	mW



OTLK: Low Power TTL Output Buffer

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
A to PAD[2]	*Rising Signal*	4340	—	7070	ps
	Falling Signal	5810	—	7280	ps
TRI to PAD (all cases)	*Rising Signal*	4960	—	8080	ps
	Falling Signal	6640	—	8320	ps
Load Dependent Delay					
A to PAD	*Rising Signal*	62	—	101	ps/pF
(for loads beyond 50pf)	*Falling Signal*	108	—	135	ps/pF
Edge Rates[2], [3]	*Rising Signal*	—	—	1	V/ns
	Falling Signal	—	—	1	V/ns
Peak Current	*Rising Signal*	—	—	55	mA
	Falling Signal	—	—	65	mA
Power Dissipation[4]		—	—	20	mW



Notes: 1) Macrocell AC performance is for user reference and is not explicitly measured.
2) With 50 pF load. 3) 0.5 - 2.4 Volts. 4) Output open circuit.

Power Disspation

The power dissipation is based on the utilization of the array's resources. The information below is meant to aid in the estimation of power dissipation. (Note: Power dissipation in the MQUAD package is limited to 2.8 Watts given the Recommended Operating Conditions specified in this data sheet.)

Power Characteristics for Array Resources:

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
P_{DOUT}	TTL output power	—	—	30	mW	*Unloaded*
P_{DOUTL}	Low power TTL output power	—	—	20	mW	*Unloaded*
P_{DIN}	TTL input power	—	—	8	mW	
P_{DINC}	CMOS input power	—	—	8	mW	
P_{DCELL}	Core cell power	—	—	0.5	mW	

Power Estimation Calculation:

Resources:

Total Signal Pads (Inputs and I/O pads)	=	92
Number of I/O Cells	=	52
Number of Input Cells	=	40
Number of Core Cells	=	2400

Calculation:

TTL/CMOS Inputs_____	x	8	= _____	mW
TTL Outputs_____	x	30	= _____	mW
Low Power TTL Outputs_____	x	20	= _____	mW
Core Cells_____	x	0.5	= _____	mW
Total Power			= _____	mW

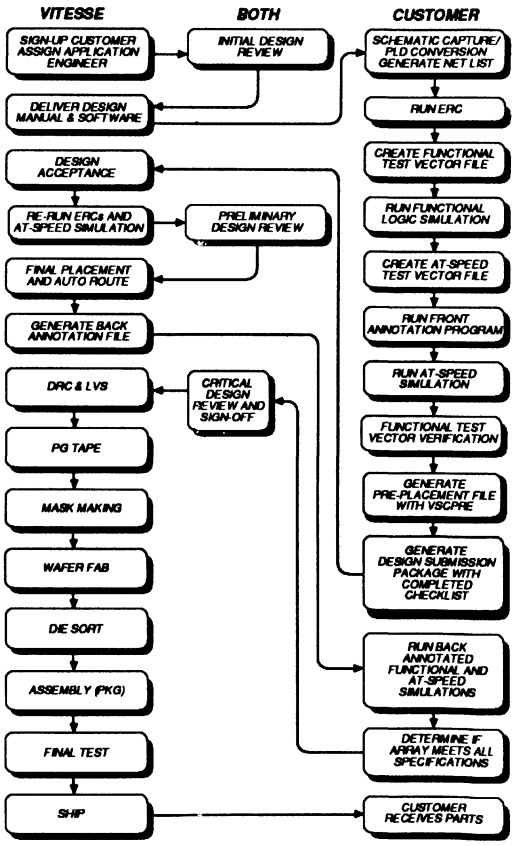
Option Development Procedure

Vitesse Semiconductor offers its customers the option of fully designing their own gate array, or having Vitesse perform a turn-key implementation of their design based on mutually agreed specifications. Regardless of the interface, a Vitesse application engineer is assigned to the customer to answer questions and track the progress of the design from start to finish. The following steps are always performed by a Vitesse application engineer.

- *Final placement and routing of the design*
- *Net-length extraction*
- *Fan-out and metal delay calculation*
- *Design rule checking and layout vs schematic*

Through experience with many gate array designs, Vitesse has created a design automation framework and a well defined flow for smooth implementation of customer designs. The flowchart at the upper right summarizes the typical gate array project flow and the various tasks delegated to the customer or to Vitesse.

Gate Array Design Flow



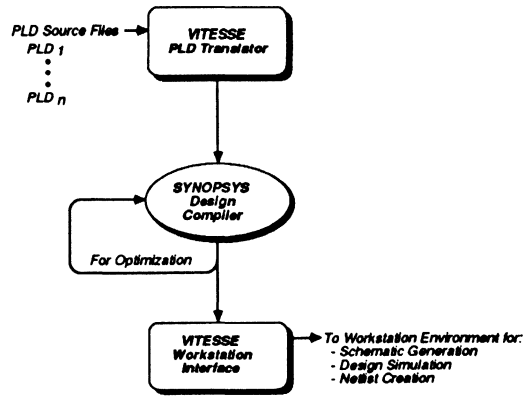
PLD Conversion Methodology

Through the use of the Synopsys Design Compiler™, Vitesse has created a direct path for the conversion of PLD source files into an optimized PLR2KT netlist. This procedure can be run at the customer site or by Vitesse and provides the necessary schematics and interconnect information for additional timing simulations as required. The PLD conversion process is outlined in the flowchart to the right.

CAD Tools/Support

PLR2KT designs are supported on MENTOR, DAISY, and VALID workstations. SYNOPSYS and VERILOG are also supported to provide logic synthesis and behavioral modeling capabilities. The Vitesse Support Package includes documentation and software which allow the customer to perform schematic capture, PLD source file conversion, functional simulation, front-annotated timing simulation, electrical rule checks, and back-annotated simulation upon completion of placement and routing. Also, Vitesse has an interactive pre-placement program that the customer may choose to use for their design.

PLD Conversion Flow



Application Note: Generation of a +2V Supply from a +5V Supply

The PLR2KT gate array requires both +2 and +5 Volt power supplies. In the event that a +2 V supply is not available in the system, a simple method exists to generate the +2 V from a +5 V supply. This method involves the use of a low cost voltage regulator. Voltage regulator ICs are offered by several vendors including National Semiconductor Corp., Linear Technology Inc., and Advanced Micro Devices.

A voltage regulator IC, such as the LT117A made by Linear Technology, is a 3 terminal device. The LT117A develops a 1.25 V reference voltage between the ***OUT*** and the ***ADJ*** terminal (see figure 1). By placing a resistor, R_1, between these two terminals, a constant current is caused to flow through R_1 and down through R_2 to set the overall output voltage. Normally this current is the specified minimum load current of approximately 5 mA. An additional current, called I_{ADJ}, flows from the ***ADJ*** terminal and through R_2. This is a very small and constant current with a magnitude of approximately 50 µA.

It can be seen from the equation in figure 1 that the accuracy of the output voltage is limited by the accuracy of V_{REF} and the tolerance of the R_1 and R_2 resistors. The LT117A has a very tight initial tolerance of V_{REF} which permits the use of relatively inexpensive 1% film resistors for R_1 and R_2 while setting an output voltage tolerance which is compatible with the PLR2KT. If voltage regulators which have wider reference tolerance are used (such as industry standard LM117), a trim pot may be needed to set the exact value of the output voltage.

Figure 2 depicts the LT117A with the resistor values needed to generate the +2 V supply. The output current of the LT117A is limited to 1.5 Amps which is sufficient for any implementation of the PLR2KT. For systems which use several PRL2KT chips, regulation can be accomplished by devices such as the LT1038 (also from Linear Technology) which can handle an output current up to 10 Amps. The use of this larger regulator is identical to the LT117A.

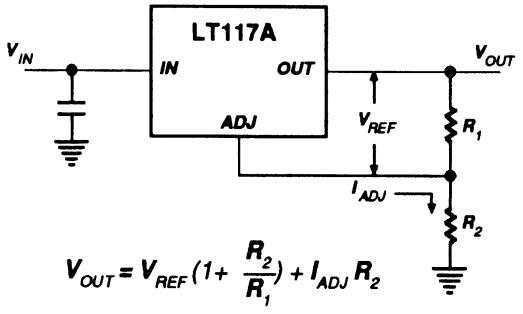


Figure 1

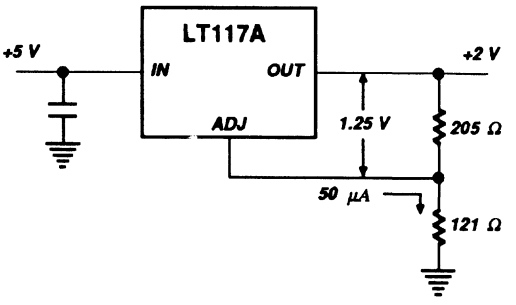


Figure 2

VSC1500/VSC1520

High Speed GaAs - 1500/1520 Gate Structured Cell Array

Features

- Superior Performance: Supports clock rates up to 2.5 GHz in Mux/Demux applications
- Proven H-GaAs E/D MESFET Process
- Array performance
  - Typical gate delay (high speed section): 150 ps @ 23 mW *(2-input XOR/XNOR, F.O. = 1, 0.5 mm wire)*
  - Typical gate delay (low power section): 330 ps @ 0.42 mW *(3-input NOR, F.O. = 1, 0.5 mm wire)*
  - High speed D Flip-flop toggle rate: > 3.3 GHz
  - Low power D Flip-flop toggle rate: 500 MHz @ 4.1 mW
  - High speed differential I/Os up to 2.5 GHz
  - ECL 100K/10KH compatible I/Os up to 400 MHz
- Structured cell approach: Array contains both high speed (SCFL) and low power (DCFL) cells to maximize performance and minimize power dissipation
- Up to 22 ECL inputs, 20 ECL outputs, 2 high speed differential inputs(1500), 3 high speed differential inputs(1520), 2 high speed differential outputs
- Power supplies: V_{EE} = -5.2 ± 0.26V, V_{TT} = -2.0 ± 0.1V
- Three temperature ranges:
  - Commercial: 0° to 70° C
  - Industrial: -40° to +85° C
  - Military: -55° to 125° C
- Power Dissipation: < 2.5W typical
- 52-pin leaded or leadless ceramic chip carrier
- Supported on MENTOR and DAISY workstations

Introduction

The VSC1500/VSC1520 are 1500 gate GaAs structured cell arrays tailored for very high speed applications in systems requiring clock rates up to 2.5 GHz. The architecture utilizes a structured cell approach that combines both high speed source coupled FET logic (SCFL) and low power direct coupled FET logic (DCFL) cells to allow the user to obtain the optimum speed/power trade-off. The speed critical sections of the design use high speed SCFL cells, while the remaining portion can be implemented with low power DCFL cells.

The VSC1500/VSC1520 are built using Vitesse's proprietary H-GaAs E/D MESFET process. The VSC1500/VSC1520 allow flexibility in design, while providing very short turnaround time (as little as six weeks) without compromising overall circuit performance.

The high speed I/O and fast internal gates make the VSC1500/VSC1520 ideally suited for mux/demux applications in fiber optic communications systems and computer backplanes. Other applications include critical paths in testers, LANs, and video graphics subsystems.

Array Architecture

The figure on page 1-26 shows the architecture of the VSC1500/VSC1520. The arrays contain input cells, output cells, high speed cells, low power cells, and translator cells. The various cell types are summarized in table 1.

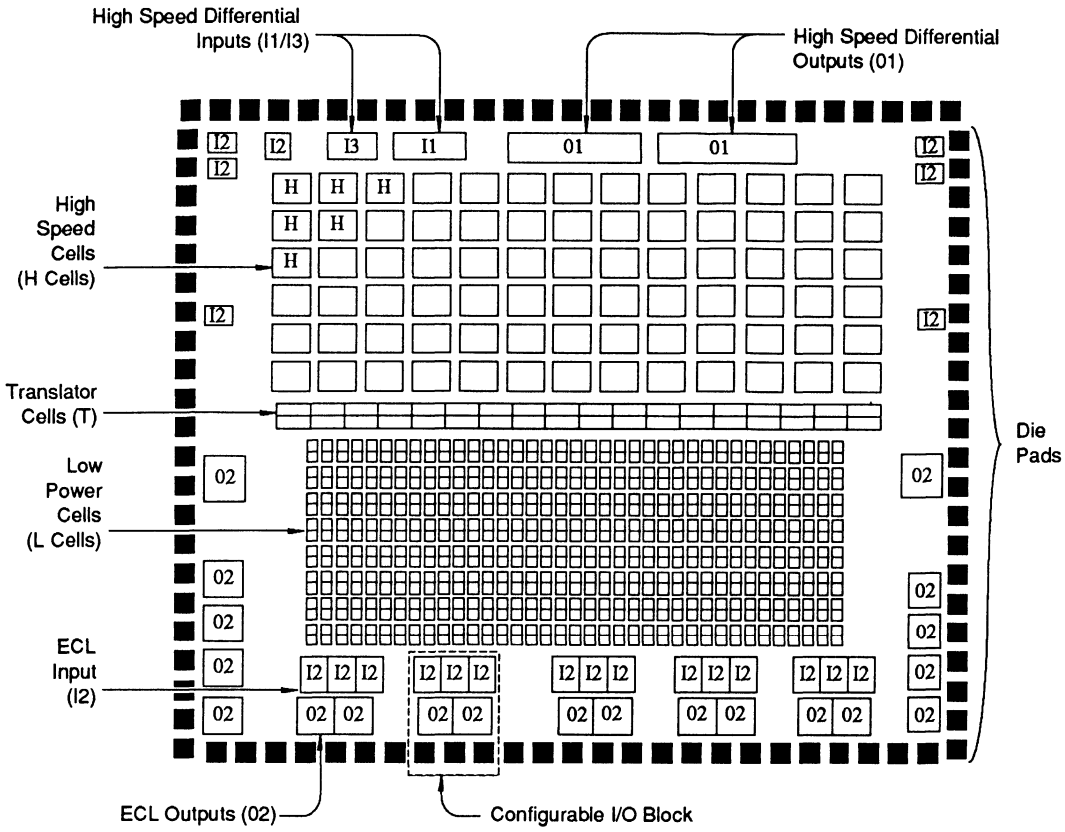
Input Cells

Input cells are used to bring signals onto the array. There are two types of input cells: high speed differential inputs, and ECL inputs.

***Table 1:** Cell Type Summary*

Input Cells	
1. High speed differential inputs(1500)	= 2
2. High speed differential inputs(1520)	= 3
3. ECL inputs	= 22
Output Cells	
4. High speed differential outputs	= 2
5. ECL outputs or	= 20
6. Differential ECL outputs	= 9
Internal Cells	
5. High speed cells	= 96
6. Low power cells	= 592
7. Translator cells	= 36

Achitecture



High Speed Differential Inputs

There are three high speed differential inputs on these arrays. These inputs are designed to bring signals on-chip at rates up to 2.5 GHz. These inputs can also be used single-ended with an on-chip reference generator. The high speed inputs accept signals with a nominal 1V peak-to-peak swing. The high speed inputs are intended to be AC coupled, therefore strict adherence to ECL input specifications is not necessary.

ECL Inputs

There are 22 ECL input cells on these arrays. These inputs accept 100K ECL levels with an on-chip reference generator. The V_{REF} input pin is used to bring external V_{BB} on chip for ECL 10K/10KH compatibility. ECL inputs can also be used as differential receivers. These inputs can be configured to yeild up to nine differential ECL receivers. These inputs can handle frequencies up to 400 MHz.

Output Cells

Output Cells are used to take signals off-chip. There are two types of output cells: high speed differential outputs, and ECL outputs.

High Speed Differential Outputs

There are two high speed differential outputs on the 1500. There are three on the 1520. These outputs are customized to take signals off-chip at rates up to 2.5 Gbits/sec. The high speed differential outputs can drive 50 ohm loads and provide a nominal 1V peak-to-peak signal swing.

ECL Outputs

There are 20 ECL outputs. These outputs can be configured to yield up to 9 differential

ECL outputs. They provide 100K ECL levels and can drive 50Ω loads. ECL outputs can handle frequencies up to 600MHz.

ECL Input and Output Cell Utilization

There are 22 ECL input cells and 20 ECL output cells. One hundred percent utilization of ECL input and output cells is not possible since ECL outputs require VCCA pads. The ECL input and output cell combinations that can be used on these arrays are shown in Table 2.

If number of ECL inputs =	22	19	16	13	10	7
then number of ECL outputs =	10	12	14	16	18	20

***Table 2:** ECL I/O Combinations*

Internal Cells

High Speed Cells

There are 96 high speed cells (H cells) which occupy about 60% of the internal core of the array. High speed cells can be used to implement speed critical portions of a design.

Each high speed cell is made up of E-mode and D-mode MESFETs and can be wired to perform a latch function. The circuit topology used is differential source coupled FET logic (similar to ECL) which results in ultra-high speed, high noise immunity macros. The H-cells use a -5.2V power supply.

Figure 2 shows a high speed cell personalized as a 2:1 multiplexer. The circuit is a two level series gated structure with a constant current generator, I_{CS}.

SB, SBN are select inputs for the mux which selects the path for the current in the lower switch. A1, A1N and A2, A2N are differential data inputs for the upper current switch. At the outputs there are two constant current source followers which provide differential logic levels for the next stage and the current gain.

Figure 3 shows the symbol for a 2:1 Mux (Macro H5). ZA, ZAN outputs and ZB,ZBN outputs are logically equivalent, but ZB,ZBN levels are shifted down by a diode drop from ZA, ZAN outputs. ZA, ZAN are for the A-inputs of the loads and ZB, ZBN are for the B-inputs of the loads.

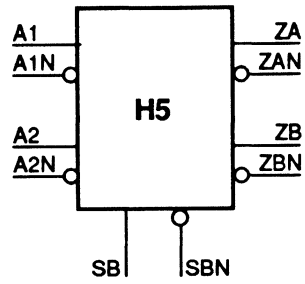


***Figure 3:** Symbol For Differential 2:1 Mux (Macro H5)*

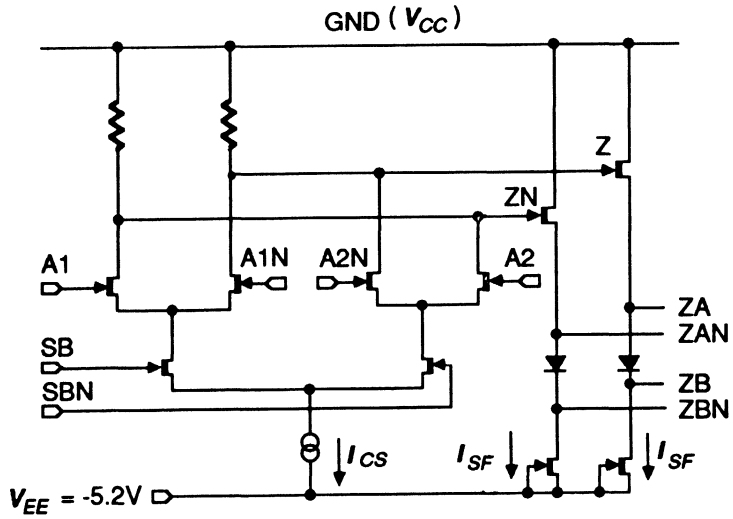


***Figure 2:** Simplified H-Cell (2:1 Multiplexer)*

Low Power Cells

There are 592 low power cells (L cells) which occupy about 35% of the internal core of the array. These cells are used to implement non-speed critical portions of a design and thus reduce overall power dissipation.

Each low power cell is made up of three enhancement mode transistors and one depletion mode transistor and can be wired to perform a 3-input NOR function. When all inputs A1, A2, and A3 are at logic 'LOW' level, output ZN is pulled HIGH. If at least one input goes HIGH, then output ZN is pulled LOW. Figure 4 below shows the schematic and symbol for a 3-input NOR (Macro L7).

The circuit configuration used is Direct Coupled FET Logic (DCFL), which provides high speed, low power macros. The low power macrocells use a -2V supply.

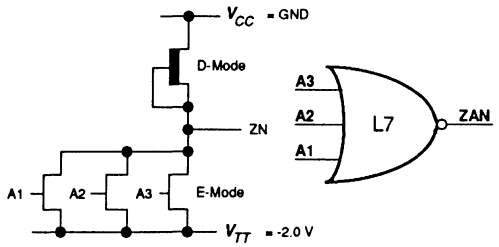


Figure 4: Schematic and Symbol For a Low Power 3-input NOR (Macro L7)

Translator Cells

There are 18 T1 translators and 18 T2 translators. T1 translators convert H-cell logic levels to L-cell logic levels. T2 translators change L-cell levels to H-cell levels. These cells occupy 5% of the internal core of the array and are located between the H-cell and L-cell sections.

Macro Library

Macros define the interconnection pattern of transistors in one or more cells which perform a logic function. A representative list of macros for the VSC1500/VSC1520 arrays are given below. For the complete set of macros, please refer to the macro library in the design manual.

High Speed Macros

- H1 - Inverter/Buffer
- H2 - 2-input OR/NOR
- H3 - 2-input AND/NAND
- H4 - 2-input XOR/XNOR
- H5 - 2:1 Multiplexer
- H6 - D-Latch
- H7 - D Flip-flop (negative edge triggered)

Low Power Macros

- L1 - High Fan-out Buffer
- L2 - Medium Fan-out Buffer
- L3 - 2-input NOR
- L4 - 2:1 Multiplexer
- L5 - D-Latch
- L6 - High Drive D Flip-flop (negative edge triggered)
- L6L - D Flip-flop (negative edge triggered)
- L7 - 3-input NOR
- L8 - 4-input NOR

Low Power Macros *(cont.)*

- L9 - 2-input XOR
- L10 - D Flip-flop with Synchronous Reset
- L11 - D Flip-flop, Asynchronous Reset & Set
- L12 - -2V Pull-down

Input Macros

- I1 - High Speed Differential Clock Input
- I2 - ECL Input
- I3 - High Speed Differential Data Input

Output Macros

- O1 - High Speed Differential Output
- O2 - ECL Output Driver

Translator Macros

- T1 - H-Cell to L-Cell Signal Translator
- T2 - L-Cell to H-Cell Signal Translator

Macrocell Performance Characteristics

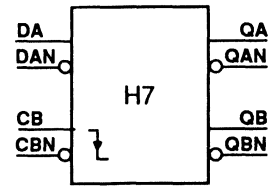
VSC1500 High Speed Macros:

(Over recommended operating conditions, Load: F.O. = 1; Ø mm wire.)

H7: D Flip-flop

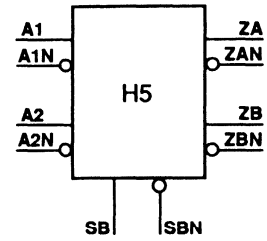
Parameter	Min	Typ	Max	Units
Propagation Delay CB, CBN to QA, QAN, QB, QBN Clock to Output	—	245	260	ps
Set-up Time	—	150	159	ps
Hold Time	—	60	64	ps
Toggle Frequency	—	2.3*	—	GHz
Power Dissipation	32	45	64	mW

* Assumes 0.5 mm wire



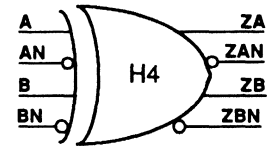
H5: 2:1 Multiplexer

Parameter	Min	Typ	Max	Units
Propagation Delay A1, A1N to ZA, ZAN, ZB, ZBN	—	175	185	ps
A2, A2N to ZA, ZAN, ZB, ZBN	—	175	185	ps
SB, SBN to ZA, ZAN, ZB, ZBN	—	235	250	ps
Power Dissipation	16	23	32	mW



H4: 2-Input XOR/XNOR

Parameter	Min	Typ	Max	Units
Propagation Delay A, AN to ZA, ZAN, ZB, ZBN	—	175	185	ps
B, BN to ZA, ZAN, ZB, ZBN	—	235	250	ps
Power Dissipation	16	23	32	mW



Load Dependednt Delay for H Cells

Parameter	Min	Typ	Max	Units
Delay/Fan-out	—	15	16	ps
Delay/mm wire	—	70	74	ps

Macrocell Performance Characteristics

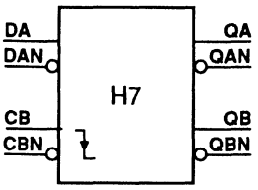
VSC1520 High Speed Macros:

(Over recommended operating conditions, Load: F.O. = 1; Ø mm wire.)

H7: D Flip-flop

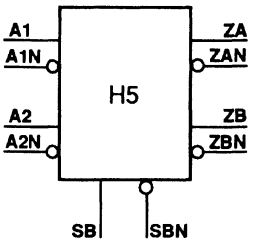
Parameter	Min	Typ	Max	Units
Propagation Delay CB, CBN to QA, QAN, QB, QBN Clock to Output	—	155	165	ps
Set-up Time	—	110	135	ps
Hold Time	—	40	50	ps
Toggle Frequency	—	3.3*	—	GHz
Power Dissipation	32	45	64	mW

* Assumes 0.5 mm wire



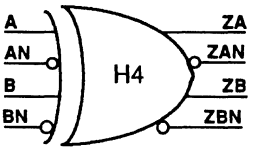
H5: 2:1 Multiplexer

Parameter	Min	Typ	Max	Units
Propagation Delay A1, A1N to ZA, ZAN, ZB, ZBN	—	115	122	ps
A2, A2N to ZA, ZAN, ZB, ZBN	—	115	122	ps
SB, SBN to ZA, ZAN, ZB, ZBN	—	145	155	ps
Power Dissipation	16	23	32	mW



H4: 2-Input XOR/XNOR

Parameter	Min	Typ	Max	Units
Propagation Delay A, AN to ZA, ZAN, ZB, ZBN	—	115	122	ps
B, BN to ZA, ZAN, ZB, ZBN	—	145	155	ps
Power Dissipation	16	23	32	mW



Load Dependednt Delay for H Cells

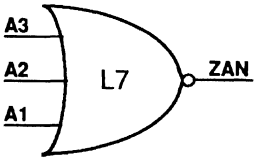
Parameter	Min	Typ	Max	Units
Delay/Fan-out	—	15	16	ps
Delay/mm wire	—	70	74	ps

VSC1500/1520 Low Power Macros:

(Over recommended operating conditions, Load: F.O. = 1; Ø mm wire.)

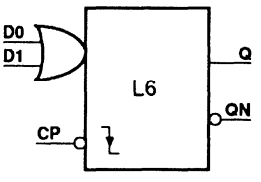
L7: 3-input NOR

Parameter	Min	Typ	Max	Units
Propagation Delay A1, A2, A3 to ZN	—	200	230	ps
Load Dependent Delay Delay/Fan-out	—	55	—	ps
Delay/mm wire	—	260	—	ps
Power Dissipation	0.28	0.42	0.56	mW



L6: High Drive D Flip-flop

Parameter	Min	Typ	Max	Units
Propagation Delay CP to Q, QN	—	560	650	ps
Set-up Time	—	530	600	ps
Hold Time	—	—	—	ps
Toggle Frequency	—	650 *	—	MHz
Load Dependent Delay Delay/Fan-out	—	30	—	ps
Delay/mm wire	—	130	—	ps
Power Dissipation	2.7	4.1	5.4	mW



* Assumes 0.5 mm wire

DC Characteristics

ECL Inputs/Outputs:

(Over recommended operating conditions with internal V_{REF}. V_{CC} = GND, Output load 50Ω to V_{TT})

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-600	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH for all ECL inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW for all ECL inputs
I_{IH}	Input HIGH current	—	10	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential ECL output pins must be terminated identically.

High Speed Inputs and Outputs:

(Over recommended operating conditions. V_{CC} = GND, Output load = 50Ω to -2.0V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for high speed inputs
V_{REF}	Input reference level	—	-3.5	—	V	
V_{OH}	Output HIGH voltage	—	-0.5	—	V	Output load, 50Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	Output load, 50Ω to -2.0 V
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output load, 50Ω to -2.0 V

NOTES: 1) Built in reference generator, the high speed inputs are designed for AC coupling.
2) If a high speed input is used single-ended, a 100pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed output pins must be terminated identically.
4) Limited ESD protection is provided for the high speed input pins, therefore, proper procedures should be used when handling this product.

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{TT}) ..... -3.0V to +0.5V
Power Supply Voltage (V_{EE}) ..... V_{CC} (GND) to -7.0V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5V to +0.5V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7V to V_{CC} + 0.7V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

Recommended Operating Conditions

ECL Power Supply Voltage (4), (V_{TT}) ..... -2.1V to -1.9V
Power Supply Voltage, (V_{EE}) ..... -5.46V to -4.94V
Operating Temperature(3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
2) V_{TT} must be applied before any input signal voltage (V_{ECLIN}) and V_{ECLIN} must be greater than V_{TT} - 0.5V.
3) Lower limit of specification is ambient temperature and upper limit is case temperature.
4) When using internal ECL 100K reference level.

Option Development Procedure

Different working relationships can be set up between the Customer and Vitesse. It may range from turn-key design to the customer doing schematic and logic simulation. The following steps in design are always done by Vitesse applications engineers.

- Placement and routing of the design
- Net-length extraction
- F.O. (fan-out) and metal delay calculation
- DRC (Design Rule Checking) & LVS (Layout vs. Schematic)

Customers who perform their own schematic capture and simulation need to have a Mentor, Daisy or Valid workstation. Vitesse provides a symbol library and simulation software for these workstations. Test vector generation and pin assignments for the design are the responsibility of the customer.

Packaging

A 52-pin multilayer ceramic leaded or leadless chip carrier is used for the VSC1500/ VSC1520. It is a cavity down package with the heat spreader on top. Particular attention has been paid to reduce crosstalk of high speed signals and to keep the trace impedance at 50 ohms.

Training

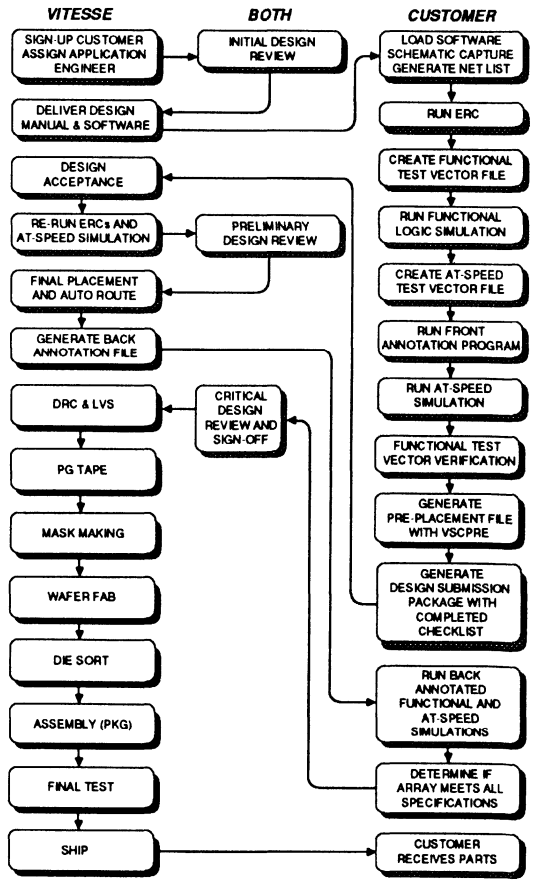
Design classes are provided to help the customer understand the gate array design process and are recommended to all customers planning to implement a design in a Vitesse gate array. These classes are three days in length and are provided at the Vitesse facility.

CAD Tools/Support

VSC1500/1520 design software is supported on MENTOR, DAISY or VALID workstations. The Vitesse Designer's Kit includes documentation and software which allows the customer to perform schematic capture, functional simulation, front-annotated timing simulation, electrical rules checks, and back annotated simulation after placement and routing are completed. Vitesse also has an interactive pre-placement program that customers may choose to use for their design.

The figure below shows the design flow for a typical gate array. Regardless of the design flow, placement and routing software is used to perform actual layout of the gate array. Once placement and routing is completed, a back annotation database is generated which represents actual metal loading. Vitesse then performs a back annotated simulation ensuring that the design will not only function correctly, but perform at the speed necessary for a successful product.

Once the critical design review and sign off are completed, Vitesse will perform a Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification. These two steps ensure that the design will work as specified. An application engineer is assigned to the customer to answer questions and track the progress of the project from start to finish.



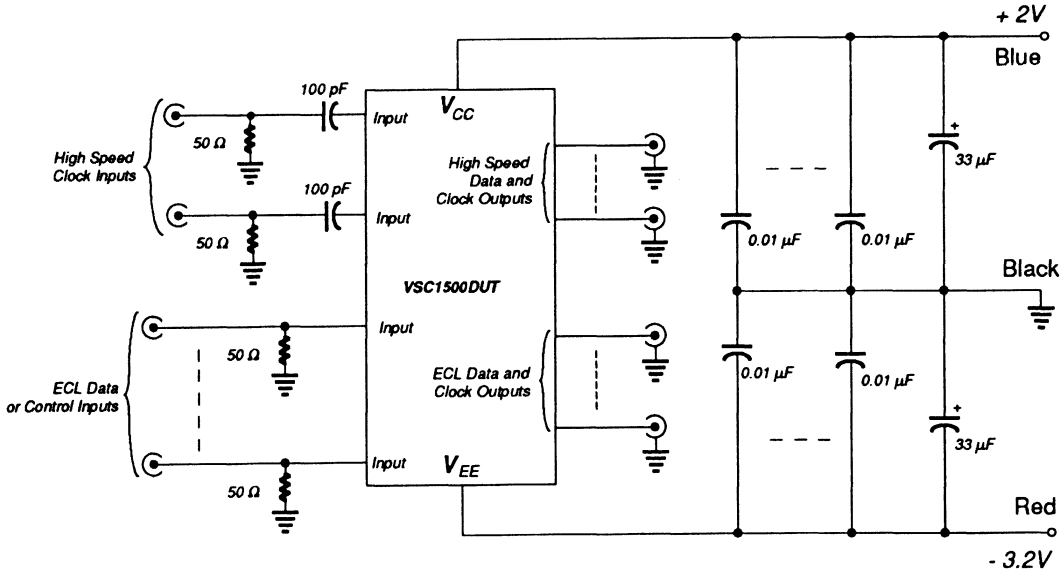
Description of the VSC1500 DUT

The VSC1500 evaluation board (VSC1500DUT) is a general purpose circuit board which provides a test bed suitable for evaluating the high performance characteristics of the VSC1500 gate array in the 52 pin leadless chip carrier. While the evaluation board is generic to the VSC1500, it can be designed with different input/output configurations for specific implementations.

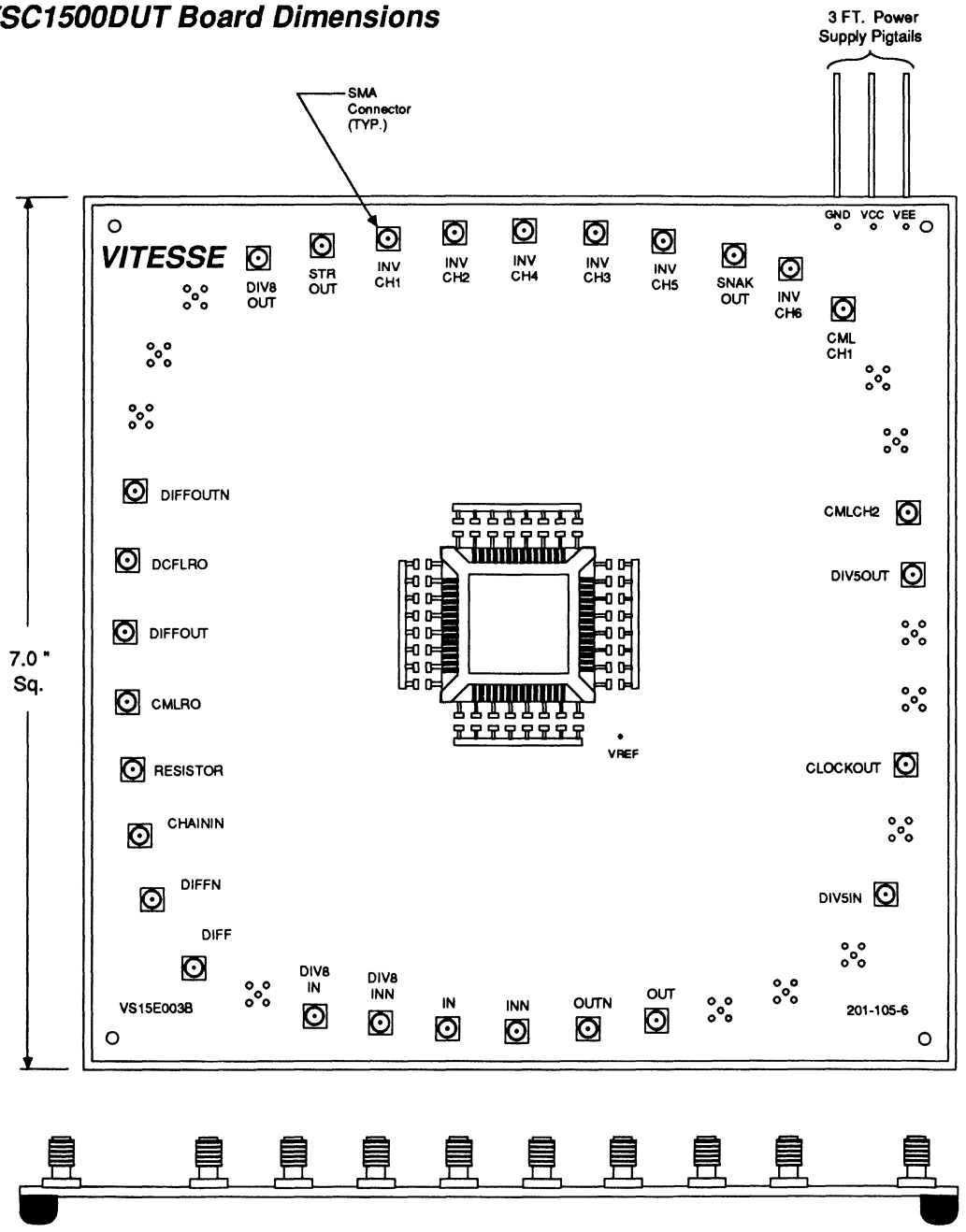
The figure below is a schematic of this circuit board. This board provides controlled impedance for all signal lines, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 100 pF blocking capacitors. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

Normally, the VSC1500 operates in an ECL environment with standard ECL power forms: ØV, -2V, -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power forms are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power form.

The device socket is an AMP 55227-1 LCC socket and was chosen for minimum inductance and shortest possible stub length. The following page shows the physical dimensions of the VSC1500 evaluation board. The figure shown is the personalization of the evaluation board for the VSC1500 gate array test chip (VSC1500TC). For further information regarding the structures which have been incorporated into the VSC1500TC, see pages 1-23 and 1-24.



VSC1500DUT Board Dimensions



VSC1500TC

High Speed GaAs -
1500 Gate Structured Cell Array Test Chip

Introduction

The VSC1500TC is a test chip personalization of the VSC1500 high speed GaAs Gate Array. This chip is packaged in a ceramic 52 pin leadless chip carrier for use in the VSC1500DUT evaluation board. Test structures utilizing high speed I/O, high speed cells, translator cells, low power cells, ECL I/O, and combinations of these have been included. The user can test speed, temperature sensitivity, power supply sensitivity, and I/O loading sensitivity by measuring these structures. All macros referred to are fully described in the VSC1500 Design Manual. The following is a description of the test structures found in the VSC1500TC.

Description of VSC1500TC Structures

DCFL Ring Oscillator (DCFLRO)

This is a 23 stage ring oscillator created from DCFL 2-input NOR gates. This 2-input NOR macro utilizes only the V_{TT} (-2.0 V) and V_{CC} (GND) supplies. For purposes of testing this structure, the V_{EE} (-5.2 V) supply may be left unconnected (The V_{EE} supply is only used for macros which are implemented in the high speed SCFL section of the array). The ring oscillator is buffered with an ECL 100K output buffer, and can drive a 50Ω load. A typical test set-up is shown in figure 1.

Loaded DCFL Inverter Chains (INVCHI - 6)

These are 6 inverter chains of 64 stages each, which are driven by a common signal. Each chain consists of a series of 64 DCFL 2-input NOR macros and one inverter macro connected to form a total of 65 inverters. The 2-input NOR macro is configured as an inverter in this structure, connecting one input low. In all 6 chains, each gate has a fan-in of 2.

The 6 chains differ in the amount and the type of loading connected at the output of each gate. The differences are described as follows:

Inverter Chain 1 (INVCH1)

This is the output from a chain of 65 low power inverters without additional loading. This structure is designed to establish the intrinsic delay characteristics of the low power 2-input NOR macro. The delay per gate derived from the measurement of this test structure should agree with the results from the ring oscillator. **Inverter chain 1** is physically near the V_{EE} sources on the chip and in combination with **Inverter Chain 6** can be used to asses the effects of backgating by comparing the performance with or without V_{EE} connected.

Inverter Chain 6 (INVCH6)

This test structure is identical in every respect to the **Inverter Chain 1** structure, with the exception of the fact that it is far from the V_{EE} sources.

Inverter Chain 2 (INVCH2)

This is the output of a chain of 65 low power inverters with every cell loaded with 0.3 mm of fully Miller capacitive metal 2 (i.e., metal 2 is an inter-digitated structure connected between the input and output of every inverter).

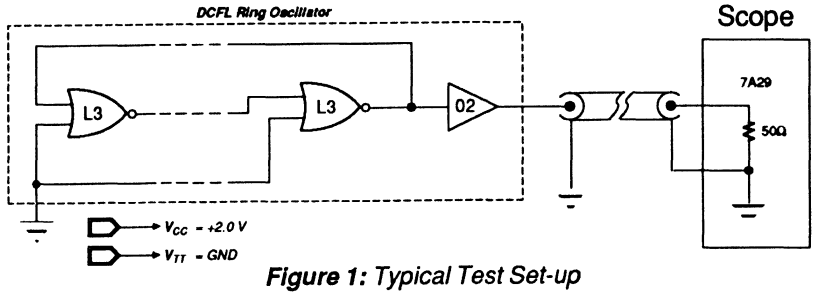


Figure 1: *Typical Test Set-up*

Inverter Chain 3 (INVCH3)

This is the output of a chain of 65 low power inverters with every other inverter loaded with 0.5 mm of metal 2 capacitance. This structure is useful in determining differences in loading effects between rising and falling edges.

Inverter Chain 4 (INVCH4)

This is the output of a chain of 65 low power inverters with every inverter connected with a load fan out of 2.

Inverter Chain 5 (INVCH5)

This is the output of a chain of 65 low power inverters with every other inverter loaded with a fanout of 3. This structure in conjunction with **Inverter Chain 4** can be used to asses the effect of fanout on rising and falling edges independently.

All the inverter chains are driven by the same external signal. The outputs are buffered by an ECL 100K output buffer. Another path, also buffered with an ECL 100K output buffer, is available that bypasses the inverter chains so that a true representation of inverter chain delays can be measured.

DCFL Divide by 5 (DIV5)

This structure is a low power (DCFL) divide by 5 circuit, composed of buffers and latches. A similarly buffered version of the clock is provided in order to accurately measure the delay through this structure. The divide by 5 output is identified as ***'DIV5OUT'*** and the buffered clock is identified as ***'CLOCKOUT'***.

DCFL Differentiated I/O Chain (DIFF-DIFF-OUT)

This structure is a differential ECL input buffer. The true and complement outputs are brought out through independent ECL output buffers. This structure can be used to evaluate the DC and AC characteristics of the VSC1500 ECL I/O buffers.

Translator Macro Chain (SNAKEOUT)

Since the VSC1500 supports two logic families: SCFL and DCFL, internal cells are required to translate logic levels between these two logic families. These macros are identified as 'T1' and 'T2' macros in the VSC1500 macro library. The 'T1' macro converts from H cell logic levels to L cell levels, while 'T2' translates from L cells to H cells. ***'SNAKEOUT'*** is the output of a chain of 13 pairs of these macros. The input stimulus is provided by ***'CHAIN IN'*** and this signal is routed back and forth between the L section and the H section. Again, the signal ***'STRAIGHTOUT'*** is available to evaluate the delay characteristics independently of the ***'CHAIN IN'*** input buffer.

Loaded SCFL Inverter Chains (CMLCH1, CMLCH2)

These structures are chains of 24 SCFL inverter cells connected in series. The inputs to this chain are provided by the stimulus ***'CHAIN IN'***. The delay through this chain (including the 'T2' and 'T1' translations) can be evaluated by comparing the output ***'CMLCHX'*** with ***'STRAIGHTOUT'***. These two chains differ as follows:

CMLCH1

This is the output of a chain of 24 SCFL inverter cells, each loaded with 1.7 mm of fully Miller capacitive Metal 1.

CMLCH2

This is the output of a chain of 24 SCFL inverter cells each loaded with 1.7 mm of fully Miller capacitive Metal 2.

SCFL Ring Oscillator (CMLRO)

This is a 23 stage ring oscillator made up of 24 SCFL inverters. The output is brought off via a T1 cell and an ECL 100K output macro.

SCFL Divide by 8 (DIV8)

This structure uses a high-speed differential input buffer to drive three sequential D Flip-flops. The output of the divide by 8 is brought out through a 'T1' cell and an ECL 100K output buffer.

High Speed I/O Chain (IN-OUT)

This structure connects a differential high speed input directly into a differential high speed output. This structure is useful in evaluating the bandwidth characteristics of the high speed I/O section of the chip.

VSC4500/VSC2000

Low Power, High Speed - LP Series GaAs Gate Arrays

Not for new designs. Replaced by VSC3K and VSC5K (see page 1-10).

Features

- Superior performance: High speed/low power
- Proven H-GaAs GaAs E/D MESFET process
- Array performance
  - Flip-flop toggle rates: 943 MHz @ 4.0 mW (typical)
  - Typical gate delay: 120 ps @ 0.34 mW (2-input NOR)
  - ECL inputs/outputs at 1 GHz
  - TTL inputs/outputs at 100 MHz
  - Typical delay-power product: ~0.03 pJ (2-input NOR)
- 100% utilization possible
- Programmable input/output interface
  - TTL or ECL (10K, 10KH, or 100K)
  - Mixed ECL and TTL
- Three temperature ranges
  - Commercial: 0° to +70° C
  - Industrial: -40° to +85° C
  - Military: -55° to +125° C
- Mil-Std-883C, level B screening and qualification available
- Fully supported on MENTOR, DAISY or VALID CAD platforms

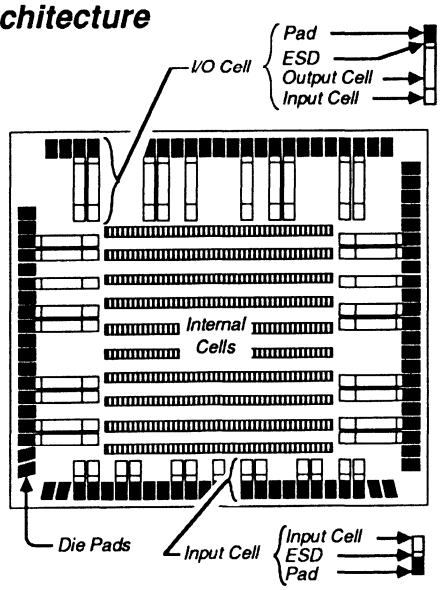
VSC2000 Specs

- Density: 1800 2-input NOR gates, or 257 D flip-flops in the core array
- I/O count: Up to 41 inputs/28 outputs; all can be ECL or TTL
- Power disspation: ~1W typical
- Packages: 52 pin Ceramic LDCC or LCC

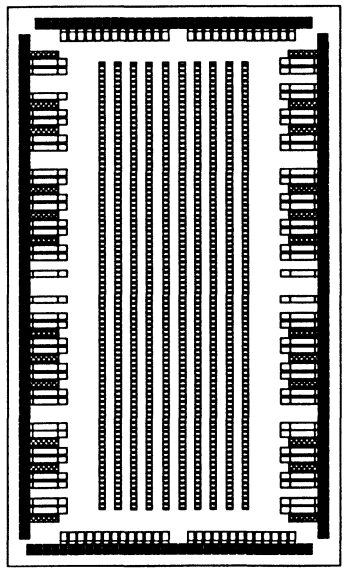
VSC4500 Specs

- Density: 4000 2-input NOR gates, or 570 D flip-flops in the core array
- Up to 120 input cells;
- all can be ECL or TTL
- Up to 68 output or bidirectional cells; all can be ECL, 48 can be TTL
- Power dissipation: 2.5W typical
- Packages: 149 pin ceramic PGA or 164 pin ceramic LDCC

Architecture



VSC2000



VSC4500

Not for new designs. Replaced by VSC3K and VSC5K (see page 1-10).

Introduction

The VSC2000 and VSC4500 are LSI ASICs suited for applications which require high levels of complexity coupled with low power state-of-the-art performance. The VSC2000 and VSC4500 are members of the LP (Low Power) Series Gate Arrays offered by Vitesse Semiconductor Corporation. Vitesse utilizes a proprietary high yielding 0.8μ GaAs enhancement/depletion MESFET process, much like silicon nMOS, to build the LP Series Gate Arrays. These arrays interface with TTL and ECL signal levels and power supplies and can easily be designed into systems utilizing these technologies without any additional system requirements. The LP Series offers the same level of performance of leading-edge ECL arrays with 1/3 to 1/4 of the power dissipation.

Applications

The LP Series can be used in a wide variety of applications including computers, workstations, communications, instrumentation, and military/aerospace systems. These arrays are intended for high performance systems requiring high speed, low power digital logic at medium to high levels of integration.

Computers

Existing mainframe systems using ECL gate arrays can improve system speed and drastically reduce power dissipation with the LP Series. The density and low power dissipation of the VSC2000 make it ideal for the consolidation of multiple PAL designs into a single chip. Systems which use standard microprocessors can bring supercomputing power to workstations by using the VSC4500. Superminicomputers can increase system performance while reducing or eliminating the need for expensive cooling systems.

Communications

Fiber optic communication links for voice or data transmission can be designed with the LP Series. These arrays offer the low power, high performance typically required in these systems while providing the high level of complexity needed to design sophisticated architectures.

Military/Aerospace

The inherent ability of GaAs devices to withstand extremes in temperature and radiation make the LP Series ideally suited for military/aerospace applications.

Architecture

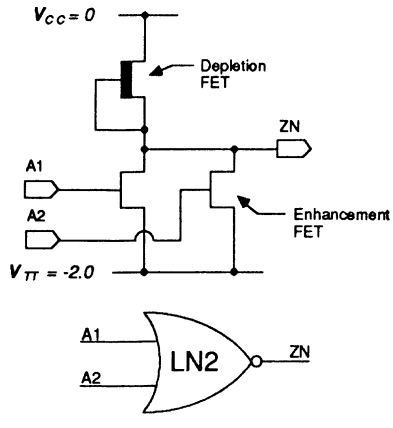
These arrays contain three basic cell types: internal logic cells, input only cells, and input/output cells which contain both input and output cells. A simplified layout of each array is shown on page 1-37.

Internal Logic Cells

The internal logic cells comprise the majority of the area of the array. The primitive element or building block is a "cell", which consists of a single depletion transistor and two enhancement transistors optimized to be configured as a 2-input NOR gate shown in the figure below. The internal arrays contain 1800 and 4000 of these cells respectively.

Input Cells

The input only cells are located along the bottom in the VSC2000 and along the bottom and top in the VSC4500 (see page 1-37). There is also an input cell in each input/output



Schematic and Symbol for a 2-Input NOR Gate

cell. Input cells can be personalized as ECL or TTL inputs or as differential to single-ended ECL inputs. TTL inputs accept standard TTL signal levels at frequencies up to 150 MHz.

ECL inputs accept standard ECL signals at up to 1 GHz. An internal reference generator is provided to ensure that adequate noise margins will be maintained under worst case conditions. Provisions are made so that the user can provide an external reference, if larger margins are desired. ECL inputs can also be used as differential receivers.

Input/Output Cells

Input/output cells are located on the top, left and right sides of the VSC2000 and on the left and right sides of the VSC4500 (see page 1-37). I/O cells contain both input and output cells and can be configured as inputs, outputs, or bidirectionals. All Input and I/O cells contain circuitry which provides ESD protection.

Output Cells

Output cells are located in input/output cells. These cells can be personalized as ECL or TTL single-ended outputs or as ECL differential outputs.

TTL outputs will provide standard TTL signal levels at frequencies up to 150 MHz. TTL outputs are available in totem pole, tri-state or open collector configurations.

ECL outputs can provide up to 1 GHz single-ended or differential 10K or 100K signal levels which can be driven across external 50Ω loads to V_{TT}. Two output drivers can be connected in parallel to provide 25Ω drive capability.

Power Supplies

The LP Series Gate Arrays can be operated in three different interface modes: a) ECL only, b) TTL only, and c) mixed ECL/TTL. The table below summarizes the power supply requirements in these various interface configurations.

I/O CONFIGURATION	*POWER SUPPLIES*
ECL Only	*-2.0 Volts and Ø Volts*
TTL Only	*+5.0, -2.0 and Ø Volts*
Mixed ECL/TTL	*+5.0, -2.0 and Ø Volts*

Not for new designs. Replaced by VSC3K and VSC5K (see page 1-10).

DC Characteristics

ECL Inputs/Outputs: *(Over recommended operating conditions with internal V_{REF}. V_{CC} = GND, Output load 50Ω to V_{TT})*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	—	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1040	—	-650	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1600	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential ECL output pins must be terminated identically.

TTL Inputs/Outputs: *(Over recommended operating conditions, TTLGND = GND)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—		V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage		—	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	—		V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage		—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

Absolute Maximum Ratings [1]

Power Supply Voltage (ECL), (V_{TT}) ..... -2.5V to +0.5V
Power Supply Voltage (TTL) (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied [2], (V_{ECLIN}) ..... +0.5V to V_{TT}
TTL Input Voltage Applied [2], (V_{TTLIN}) ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HIGH) ..... 50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

2) V_{TT} (V_{TTL}) must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.

Recommended Operating Conditions

ECL Power Supply Voltage [1], (V_{TT}) ..... -2.1V to -1.9V

TTL Power Supply Voltage, (V_{TTL}) ..... +4.75V to +5.25V

Operating Temperature [2], (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTE: 1) When using internal ECL 100K reference level.

2) Lower limit of specification is ambient temperature and upper limit is case temperature.

Packaging

The VSC2000's standard package is a 52-pin ceramic leaded (LDCC) or leadless (LCC) chip carrier. The VSC4500 may be packaged in a 149 pin ceramic pin grid array (PGA) or a 164 pin ceramic leaded chip carrier (LDCC). All three packages are multilayer ceramic packages with the cavity down and a Cu-W heat spreader on top. Particular attention has been paid to reduce crosstalk of high speed signals and to keep the trace impedance at 50Ω.

VCB50K

Standard Cell Library

Features

- VLSI complexity: > 50,000 gates
- Superior performance: 300 MHz to 3 GHz
- Choice of operating temperature ranges:
  - Commercial: 0 to 70 °C
  - Industrial: -40 to 85 °C
  - Military: -55 to 125 °C
- ECL, GaAs, or TTL compatible inputs/outputs
- Choice of input/output interfaces
  - TTL
  - ECL (10K, 10KH, or 100K)
  - GaAs
  - Mixed (TTL, ECL, and GaAs)
- VLSI Technology™, Inc. design tools supported
- Supported on MENTOR and VALID platforms
- VERILOG XL™ behavior modeling and simulation
- Synopsis logic synthesis tools supported
- Very low power dissipation
- High yield, 4 layer metal, VLSI process
- Mil-Std-883C, Level B screening and qualification available
- Customized megacell capability
- Very low sensitivity to total dose radiation
- Complete family of high pin count ceramic and MQuad™ packages

GaAs Cell Based Design

GaAs integrated circuits provide superior performance when either speed or power are the critical design parameters. High performance GaAs ICs have traditionally been implemented with a full custom design approach. Cell based design techniques offer flexibility and performance similar to full custom implementations, but with a front-end design technique identical to that of a gate array. In addition, the use of a predefined library of tested, fully characterized cells increases the probability of a first pass success.

The Vitesse VCB50K Standard Cell Library is an extensive collection of cells suitable for implementing complex logic designs. The elements of the library include simple gates, flip-flops, adders, multiplexers, decoders and input/output buffers. Multiple speed-power versions of each cell are provided to optimize a design. Logic and timing simulation models of each cell are provided for logic simulation of circuit performance. A companion library includes Megacells (RAM, ROM, ALU, ect.) which allow a designer to easily implement complex designs on a single chip.

The VCB50K standard cell library has been optimized for performance at clock rates of 300 MHz to 3 GHz. This has been accomplished by implementing the cells using direct coupled FET logic (DCFL) and source-coupled FET logic (SCFL). The DCFL versions of the cells operate at clock speeds in excess of 1 GHz and consume very little power. The SCFL cells are suitable for up to 3 GHz operation.

The VCB50K library contains both core and pad cells. DCFL and SCFL libraries are provided for both commercial and military temperature ranges.

DCFL cells have a fixed height of 72μm for optimized placement and routing using VLSI's Chip Compiler. The DCFL cell width is variable and depends on complexity. Signal connectors are available on both the top and bottom of DCFL cells for improved routing efficiency. Power busses are on a fixed grid to facilitate abutting adjacent cells.

The SCFL cell library (referred to in the VCB50K manual as the VCBHSC library) also contains both core and I/O cells. Basic SCFL cells have a fixed height of 230μm. The width for most functions is 120μm. A high-speed D flip-flop is 240 μm wide. I/O pad cells are available for both core limited and pad limited designs. The I/O cells are tall and narrow to

minimize the circumference of the pad ring for pad limited designs.

Direct-Coupled FET Logic (DCFL)

VLSI levels of integration can be achieved in GaAs via direct-coupled FET logic ICs. DCFL uses a minimum number of active devices per logic function. The result is minimal power dissipation and high packing density. The circuitry operates by current steering, therefore, most of the power dissipated is static power. For high speed switching circuits. In addition, power supply noise caused by large current transients is eliminated.

A DCFL inverter, the simplest logic element in DCFL, consists of one enhancement mode and one depletion mode transistor. The depletion mode transistor is a constant current load and the enhancement mode MESFET acts as a switch. Current from the load is steered through the pull down switch or to the gate terminal of the succeeding switch.

DCFL is tolerant to large variations in power supply voltage. Due to the characteristics of the load device, full switching speed can be achieved with a supply voltage as low as 1.25V. A -2V supply is used because this is the standard ECL termination supply (V_{TT}), and simplifies the interface with ECL I/O.

A critical factor which determines the performance of complex DCFL circuits is the uniformity of transistor threshold voltage (V_{TH}). Vitesse has carefully optimized the wafer fabrication process to minimize V_{TH} variations. The process is currently capable of producing chips with over 300K gates at reasonable yields.

Another advantage of GaAs DCFL technology is that the performance improves as the temperature increases. Power dissipation of DCFL is independent of logic state or frequency of operation.

Source-Coupled FET Logic (SCFL)

Ultra high speed logic functions can be implemented using source-coupled FET logic (SCFL) cells. The circuit topology of SCFL is very similar to ECL as shown in Figure 1. High speed performance is obtained by using only depletion mode transistors. The power dissipated by an SCFL gate is much greater than an equivalent gate implemented in DCFL, however, a 2x to 4x speed improvement is obtained. SCFL is the circuit topology of choice when ultra-high speed performance is required.

All SCFL circuits include source-follower output buffers. Two levels of series gating are performed in the switch pairs, and the source

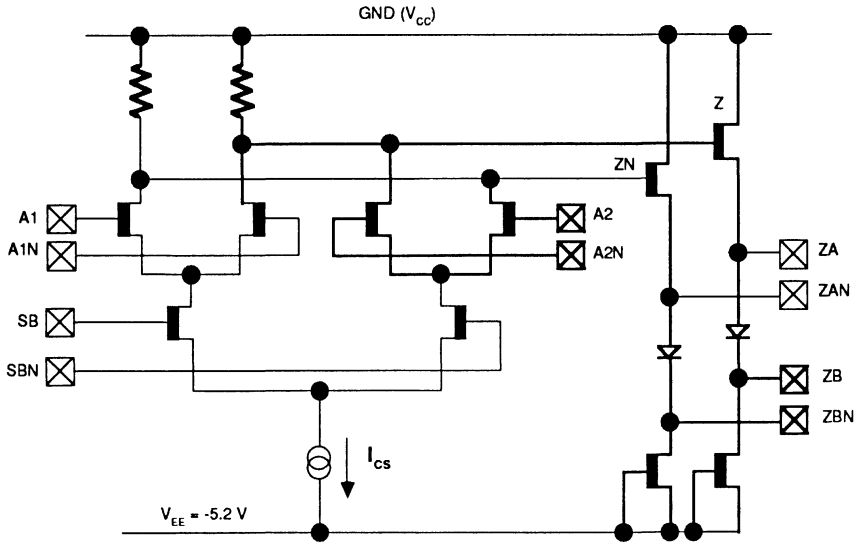


Figure 1: *SCFL Differential 2:1 Multiplexer (H21MM1/H21MM2)*

Package	Part Name	Number of I/O's (Max Output)	Equivalent Gates in Core**
22 Pin DIP	DP22A-C	20*	500-1500
24 Pin DIP	DP24A-D	22*	500-2000
28 Pin LDCC	LD28A-E LL28A-E	26*	500-2250
52 Pin LDCC	LD52A-G LL52A-G	41*	500-5000
52 Pin MQUAD	MQ52A-H	50*	500-5000
132 Pin LDCC	LD132H	92(52)	6000
149 Pin PGA	PG149I	120(68)	10,000
164 Pin LDCC	LD164I	120(68)	10,000
211 Pin PGA	PG211J	174(100)	25,000
256 Pin LDCC	LD256J	196(100)	25,000
344 Pin LDCC	LD344K	256(156)	50,000

* These packages do not have dedicated "dirty" supply pins for output transparent currents. Some pins will have to be used for this purpose. This number depends on the number of outputs.
** This number may decrease significantly in designs with high total cell pin count.

Table 2: *VCB50K Standard Packages*

followers serve as level shifters. The differential switching portion consists of a constant current source, I_{CS} and two levels of differential current switches, A and B, forming a series gated structure. The select signal pair (SB, SBN) form the lower level current switch. Input signal pairs (A1, A1N and A2, A2N) form the upper level current switch. Select inputs (SB, SBN) determine which switch pair (A1 or A2) I_{CS} flows through.

The outputs are constant current sources, with Z and ZN transistors providing current gain for the outputs. There are two pairs of differential outputs (ZA, ZAN and ZB, ZBN). The ZB, ZBN output is logically equivalent to ZA, ZAN, but is shifted down by one diode drop. This facilitates the interconnection of SCFL cells. The signal levels compatible with the upper level switch are generated at ZA, ZAN. Signal levels compatible with the lower level switch are generated at ZB, ZBN. Depending on the load cell, the proper output is selected to

Die Name	Die Size (Mils)	Die Size (mm)	Available Core Area (est.)	Equivalent Core Gates (est.)
A	85 X 96	2.16 x 2.45	0.89 x 1.49	500
B	113 X 96	2.88 x 2.45	1.92 x 1.18	1000
C	113 X 125	2.88 x 3.18	1.61 x 2.2	1500
D	113 X 144	2.88 x 3.68	1.61 x 2.72	2000
E	130 X 130	3.3 x 3.3	2.34 x 2.03	2250
F	170 X 144	4.33 x 3.68	3.37 x 2.72	3500
G	170 X 170	4.33 x 4.33	3.37 x 3.06	5000
H	260 X 145	6.6 x 3.68	5.33 x 2.72	6000
I	289 X 170	7.35 x 4.33	6.39 x 2.61	10,000
J	289 X 340	8.65 x 7.35	7.69 x 6.08	25,000
K	542 X 304	13.78 x 7.73	12.74 x 6.46	50,000

Table 3: *Die Sizes and Equivalent Gates*

make the signal levels compatible.

SCFL circuits require a ±5.2 V supply compared to the -2 V used for DCFL. Since the signal levels in the two logic families are different, the VCB50K Library includes level translator cells which enable communication between them. These translator cells allow DCFL and SCFL logic to be combined on a single chip.

Tables 2 and 3 show the standard packages offered for VCB50K designs as well as the standard die sizes. The user should note that the possible die sizes for each package are indicated in the suffix of the part name.

Design Tools

The VCB50K library is compatible with the VLSI Technology, Inc. tool set. In addition, designs are supported on Mentor and Valid platforms. High level design approaches are accommodated through Verilog and Synopsys.

The user may choose to implement their circuit using an automated or an interactive design approach. In the automatic approach, schematic capture, simulation and netlist/test vector generation are the major design tasks. In addition, cell placement and routing is automatically performed. The interactive approach is recommended for the experienced designer who requires optimum performance. In the interactive mode, the designer may manually place and route critical paths and include custom circuitry in the design.

Schematic capture and full timing simulation are supported on Mentor and Valid platforms. The user interface is almost identical to that used for gate array design development. The designer creates the schematics, performs functional and front-annotated simulation, and delivers the netlist and test vectors to Vitesse. Vitesse implementation engineers then perform placement and routing and provide back annotation data for resimulation at the customer's site. The design is then released to Vitesse for prototype fabrication.

Custom Cells

Vitesse will develop custom cells of any complexity to customer specifications or a designer may construct custom cells to be included in the library by following the cell development guidelines.

VCB50K - Standard Cell Library

The following is a summary of the cells currently available in the library. Virtually all functions are available in commercial and military operating temperatures and offer a range of signal buffering strengths. Performance characteristics for selected cells are given on the following pages. For a complete listing and specifications, refer to the Design Manual.

ADDERS
1-Bit Full Adder
2-Bit Full Adders

BUFFERS
GaAs Buffer
Inverting Buffers
Dual Inverting Buffer
Non-Inverting Buffers

COMPARATORS
5-Bit Comparators

DECODERS
2:4 Decoders
2:4 Decoders with Enable

ECL INPUT/OUTPUT BUFFERS
Bidirectional ECL Input/Output Buffer
Dual 25Ω Bidirectional ECL Input/Output Buffer
Bidirectional TTL Input/Output Buffers
ECL Input Buffers
Single-Ended to True and Complement ECL Input Buffer
ECL Input Buffer with Dual Outputs
Inverting ECL Input Buffer

***ECL INPUT/OUTPUT BUFFERS** (cont.)*
Differential to Single-Ended ECL Input Buffers
Differential ECL Input Buffer with Dual Outputs
ECL Output Buffer
25Ω ECL Output Buffer
Single-Ended to True and Complement ECL Output Buffer
25Ω ECL Cut-Off Output Buffer

FLIP-FLOPS
D Flip-Flop with Preset and Clear
D Flip-Flop with Clear
D Flip-Flop with Q & QN Outputs
D Flip-Flop with Q Output Only
Multiplexed D Flip-Flop with Clear

GaAs INPUT/OUTPUT BUFFERS
GaAs Input Pad
50Ω GaAs Output Buffer

GATES
4-Input AND Gates
2/2-Input AND-OR-Invert Gates
2-Input NAND Gates
2-Input NOR Gates

***GATES** (cont.)*
3-Input NOR Gates
4-Input NOR Gates
2/2 OR-AND-Invert Gates
2/1 OR-AND-Invert Gates
4-Input OR Gates
2-Input XNOR Gates
2-Input XOR Gates

LATCHES
Latches
Latch with 2-input OR Gate Input
Scan Registers

MULTIPLEXERS
4-to-1 Multiplexers with Enable
2-to-1 Multiplexers
4-to-1 Multiplexers

MISCELANEOUS
Active High Pull Up
Pull Down

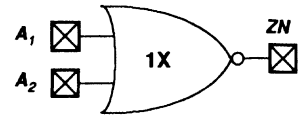
TTL INPUT/OUTPUT BUFFERS
TTL Input Biffer
TTL Output Buffer

Selected Macrocell AC Performance Characteristics

(V_{TT} = -2.0V, V_{CC} = V_{CCA} = GND, T_C = 25° C, Load: F.O. = Ø; Ø mm wire.)

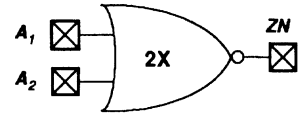
NR02D1: 2-Input NOR Gate

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to ZN	*Rising Signal*	74	—	121	ps
	Falling Signal	100	—	125	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	57	—	90	ps
	Falling Signal	17	—	22	ps
Delay/mm wire	*Rising Signal*	192	—	313	ps
	Falling Signal	48	—	61	ps
Power Dissipation		—	0.6	0.8	mW



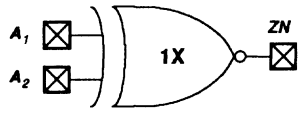
NR02D2: Buffered 2-Input NOR Gate

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to ZN	*Rising Signal*	50	—	81	ps
	Falling Signal	83	—	104	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	28	—	46	ps
	Falling Signal	11	—	14	ps
Delay/mm wire	*Rising Signal*	96	—	157	ps
	Falling Signal	31	—	39	ps
Power Dissipation		—	1.0	1.6	mW



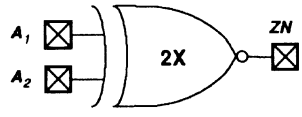
XN02D1: 2-Input XNOR Gate

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to Z	*Rising Signal*	130	—	293	ps
	Falling Signal	158	—	302	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	56	—	91	ps
	Falling Signal	16	—	20	ps
Delay/mm wire	*Rising Signal*	192	—	313	ps
	Falling Signal	45	—	57	ps
Power Dissipation		—	2.7	4.0	mW



XN02D2: Buffered 2-Input XNOR Gate

Parameter		Min	Typ	Max	Units
Propagation Delay					
A1, A2 to Z	*Rising Signal*	136	—	273	ps
	Falling Signal	199	—	374	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	28	—	46	ps
	Falling Signal	11	—	14	ps
Delay/mm wire	*Rising Signal*	96	—	157	ps
	Falling Signal	32	—	40	ps
Power Dissipation		—	3.1	4.7	mW

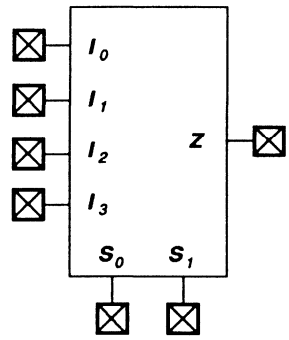


Selected Macrocell AC Performance Characteristics (continued)

(V_{TT} = -2.0V, V_{CC} = V_{CCA} = GND, T_C = 25° C, Load: F.O. = Ø; Ø mm wire.)

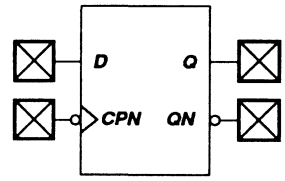
MX41D1: 4:1 Multiplexer

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
S0, S1 to Z	*Rising Signal*	161	—	434	ps
	Falling Signal	224	—	426	ps
I0 - I3 to Z	*Rising Signal*	167	—	273	ps
	Falling Signal	224	—	281	ps
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	56	—	91	ps
	Falling Signal	17	—	22	ps
Delay/mm wire	*Rising Signal*	192	—	313	ps
	Falling Signal	48	—	61	ps
Power Dissipation		—	3.9	5.6	mW



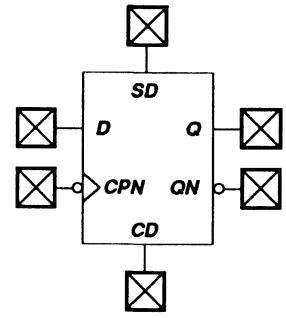
DFN1D2: Negative Edge Triggered D Flip-flop with Q & QN Outputs

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
CPN to Q	*Rising Signal*	267	—	434	ps
	Falling Signal	340	—	426	ps
CPN to QN	*Rising Signal*	198	—	323	ps
	Falling Signal	324	—	406	ps
t_{SET-UP}		—	190	—	ps
t_{HOLD}		—	210	—	ps
Toggle frequency (assumes 0.25 mm wire)		1.3	—	1.6	GHz
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	15	—	27	ps
	Falling Signal	13	—	19	ps
Delay/mm wire	*Rising Signal*	52	—	94	ps
	Falling Signal	37	—	54	ps
Power Dissipation		—	5.5	8.1	mW



DFB0D2: Negative Edge Triggered D Flip-flop with Preset & Clear

Parameter		*Min*	*Typ*	*Max*	*Units*
Propagation Delay					
CPN to Q	*Rising Signal*	397	—	646	ps
	Falling Signal	266	—	333	ps
CPN to QN	*Rising Signal*	310	—	505	ps
	Falling Signal	365	—	458	ps
CD to Q	*Falling Signal*	374	—	468	ps
CD to QN	*Rising Signal*	174	—	283	ps
SD to Q	*Rising Signal*	180	—	293	ps
SD to QN	*Falling Signal*	382	—	478	ps
t_{SET-UP}		—	240	—	ps
t_{HOLD}		—	100	—	ps
Toggle frequency (assumes 0.25 mm wire)		1.2	—	1.5	GHz
Load Dependent Delay					
Delay/Fan-out	*Rising Signal*	17	—	27	ps
	Falling Signal	14	—	19	ps
Delay/mm wire	*Rising Signal*	58	—	94	ps
	Falling Signal	41	—	54	ps
Power Dissipation		—	5.6	8.8	mW



DC Characteristics

TTL Inputs/Outputs: *(Over recommended operating conditions, TTLGND = GND)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	V_{TTL}	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	—	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	—	V_{TTL}	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	V_{IN} = V_{TTL} - 0.5 V
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OCZ}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

ECL Inputs/Outputs: *(Over recommended operating conditions with internal V_{REF}. V_{CC} = V_{CCA} = GND, Output load 50Ω to -2.0V)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	V_{IN} = V_{IH} max
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} min

Note: 1) Differential ECL output pins must be terminated identically.

GaAs Inputs/Outputs: *(Over recommended operating conditions, V_{CC} = V_{CCA} = GND, Output load 50Ω to -2.0V)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	V_{TT}+1000	—	V_{TT}+1400	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	V_{TT}+150	mV	
V_{IH}	Input HIGH voltage	V_{TT}+775	—	V_{TT}+1200	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	V_{TT}+375	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	V_{IN} = V_{IH} max

Note: 1) Differential GaAs output pins must be terminated identically.

DC Characteristics *(continued)*

High Speed SCFL Inputs/Outputs: *(Over recommended operating conditions, V_{CC} = 0V, T_C = 25°C)*

Parameters	Description		Units	Conditions
Input Receiver (HIEDM5; HCKDM0):				
V_{REF}	Reference voltage	-3.5 +1.5	V V	V_{EE} = -5.2V±0.26V V_{EE} = +5.0V±0.25V
V_{PP}	Peak to peak swing	800-1000	mV	
Output Driver (HOEDM5):				
V_{REF}	Reference voltage	-1.2 +3.8	V V	V_{EE} = -5.2V±0.26V V_{EE} = +5.0V±0.25V
V_{PP}	Peak to peak swing	800-1000	mV	

Both true and complementary signals must be terminated with 50 Ω to V_{TT} (-2V for negative voltage SCFL or to +3V for positive voltage SCFL).

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{TT}) ..... -2.5V to +0.5V
Power Supply Voltage for Negative Voltage SCFL (V_{EE}) ..... -6.0V to +0.5V
Power Supply Voltage for Positive Supply SCFL/TTL (V_{EE}) ..... +6.0V to -0.5V
Power Supply Voltage (TTL) (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... +0.5V to V_{TT}
TTL Input Voltage Applied (2), (V_{TTLIN}) ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HIGH) ..... 50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

2) V_{TT} (V_{DD}) must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.

Recommended Operating Conditions

ECL Power Supply Voltage (1), (V_{TT}) ..... -2.1V to -1.9V
TTL and Positive Voltage SCFL Power Supply Voltage, (V_{TTL}) ..... +4.75V to +5.25V
SCFL Power Supply Voltage(3), (V_{EE}) ..... -5.2V to ±0.26V
Operating Temperature (2), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTE: 1) When using internal ECL 100K reference level.
2) Lower limit of specification is ambient temperature and upper limit is case temperature.
3) When using negative voltage SCFL.

Design Flow

The following section describes the five phases in a typical design flow.

Design and Specification Submission

The customer captures schematics and performs logic and timing simulations using the Vitesse VCB50K library on Vitesse supported CAE workstations. A documentation package is submitted to Vitesse which describes the specifications of the chip. The submission package must include the workstation netlist files, the simulation vector set (stimulus and

response), and any other design, test, quality assurance, and manufacturing requirements applicable to the development.

Preliminary Design Review

The customer and Vitesse mutually review the submission package. Vitesse verifies that all documentation is completed and performs checks for design feasibility. After the review, Vitesse re-simulates the circuit and provide written notification of design acceptance. Any items which may impact the scheduled milestones or require the customer to re-submit a corrected submission package are noted.

Vitesse Design and Layout

After the design is accepted, Vitesse will design and layout the chip based on the information contained in the submission package. This includes running Electrical Rule Checks (ERCs) and up to two passes of placement and routing. For each iteration of placement and routing the customer will re-run back-annotated simulations of the circuit using actual metal delays. The customer must sign off that the design meets the performance standards desired for the device before mask and wafer fabrication are started. Vitesse also provides pinouts at this time if they were not previously defined.

Critical Design Review

Vitesse and the customer review and approve the entire set of simulation results, pin-out requirements, and testing procedures.

Shipment of Initial Prototypes

After customer approval and authorization to proceed, Vitesse fabricates and tests the initial prototype devices. This includes a final ERC, LVS layout verification, generation of a PG tape, mask fabrication, wafer fabrication, assembly, and shipment of initial samples temperature-tested to the documented specifications. Vitesse will create a standard test program based on generic program files and the customer supplied simulation/test patterns. This test program includes parametric tests, functional tests, and any other optional tests, such as AC critical path delay measurements. If necessary, the customer will provide any additional timing information which is required.

VS8001/VS8002

12:1 Multiplexer - 1:12 Demultiplexer Chip Set

Features

- Serial data: up to 1.25 Gb/s
- ECL 100K/10KH compatible parallel data inputs/outputs
- Set input on VS8001 synchronizes external and internal clocks
- Skip input on VS8002 for alignment of 12-bit output to word boundaries
- Standard ECL power supplies: V_{EE} = -5.2 V ± 0.26 V, V_{TT} = -2.0 V ± 0.1 V
- Available in commercial or industrial temperature ranges

Functional Description

Introduction

The VS8001 and VS8002 are high speed data conversion devices capable of serial data rates up to 1.25 Gb/s, transforming 12-bit wide parallel data to serial data and serial data to 12-bit wide parallel data. Evaluation of the parts is facilitated by on-chip self-test circuitry.

The VS8001/VS8002 is fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leadless or leaded chip carrier. Refer to Section 6, "Packaging" for a complete description of these packages.

VS8001

The VS8001 is a 12-bit parallel to serial data converter. A fully synchronous internal design receives 12 parallel single-ended ECL bit streams ***(D_0 - D_{11})*** and converts these to a single differential bit stream ***(MUXDATA, NMUXDATA)*** up to 1.25 Gb/s. To accommodate various system timing constraints, both the high frequency clock ***(CLK, NCLK)*** and low frequency divide by 12 clock ***(CLOCK12)*** are driven off chip. A synchronizing input ***(SET)*** allows alignment of the internal low-frequency clock to an externally supplied clock ***(DCLOCK)***.

VS8002

The VS8002 is a serial to 12-bit parallel data converter. A fully synchronous internal design receives a single bit stream ***(MUXDATA, NMUXDATA)*** operating at data rates up to 1.25 Gb/s and converts it to 12 parallel single-ended ECL bit streams ***(D_0 - D_{11})***. The high frequency clock ***(CLK, NCLK)*** is externally supplied. The low frequency divide by 12 clock ***(DCLOCK)*** is driven off chip synchronous with the parallel data. An external signal ***(SKIP)*** may be used to slip the low frequency clock by one serial data bit for alignment of the 12-bit output to word boundaries. A ***SKIP*** input causes output to be invalid for up to 3 ***DCLOCK*** cycles.

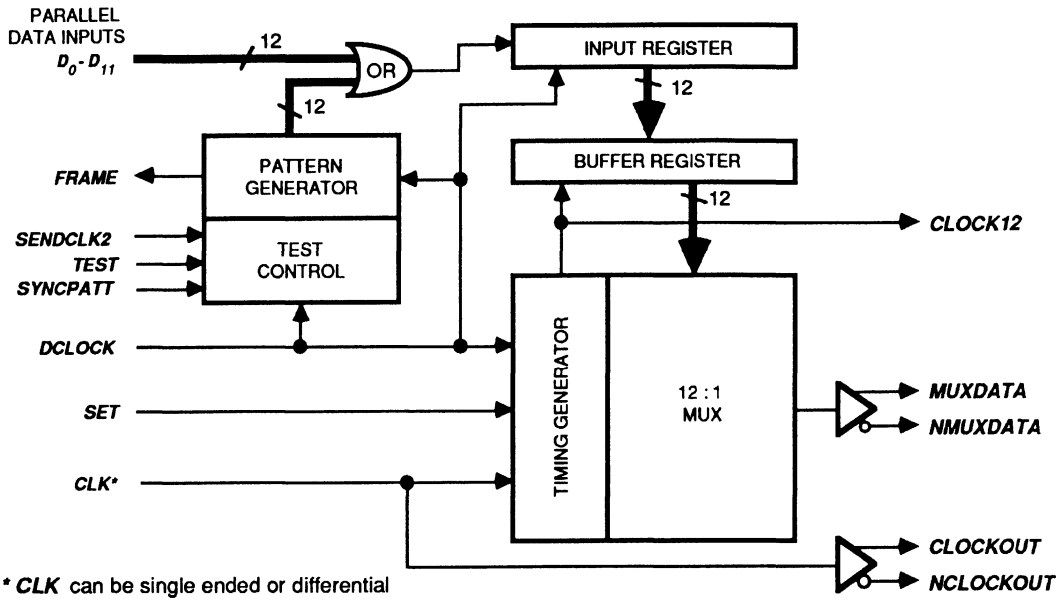
Self-Test Feature

In addition to normal parallel to serial and serial to parallel data conversion hardware, the VS8001 and VS8002 contain features which allow the user to fully evaluate the at-speed functionality of the devices. Given some simple enabling signals ***(TEST, SYNCPATT)***, built in hardware causes the VS8001 to transmit multiplexed internally generated data patterns via its high speed serial port to the high speed serial input on the VS8002. These signals allow the VS8002 to align itself to word boundaries and compare incoming data to its own internally generated, pseudo-random test patterns. Test enabling pins on the VS8002 consist of the ***TEST*** and ***SYNCPATT***. Test is confirmed on the ***ALIGNED, ERROR, FRAME*** and ***MATCH*** pins on the VS8002.

Applications

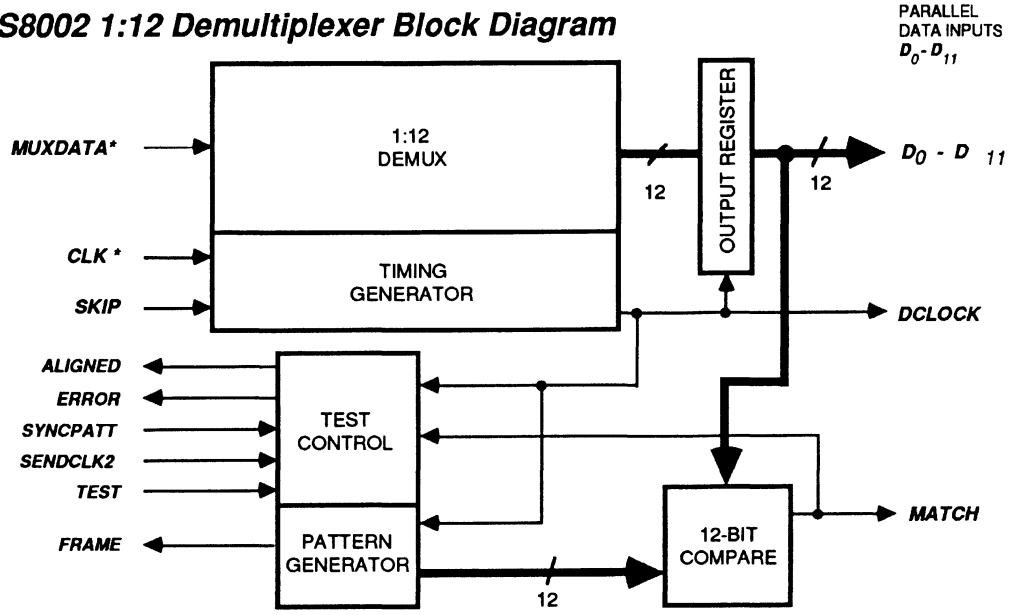
- High speed instrumentation and test equipment
- Fiber optic communication
- Local area networks
- Serialization of computer backplanes
- Computer to computer interfaces
- Serial control buses for aerospace environments

VS8001 12:1 Multiplexer Block Diagram



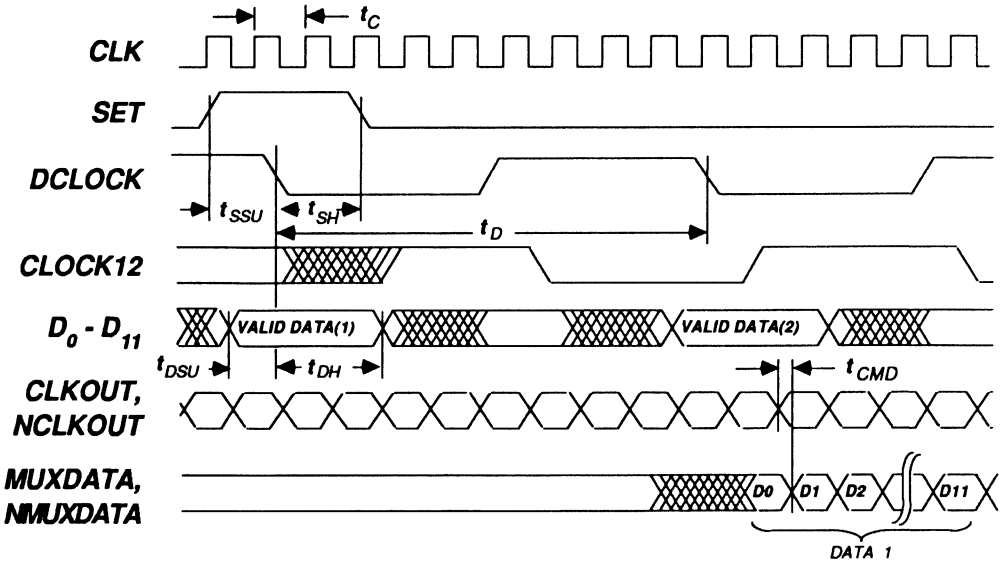
* ***CLK*** can be single ended or differential

VS8002 1:12 Demultiplexer Block Diagram



* ***MUXDATA*** and ***CLK*** can be single ended or differential

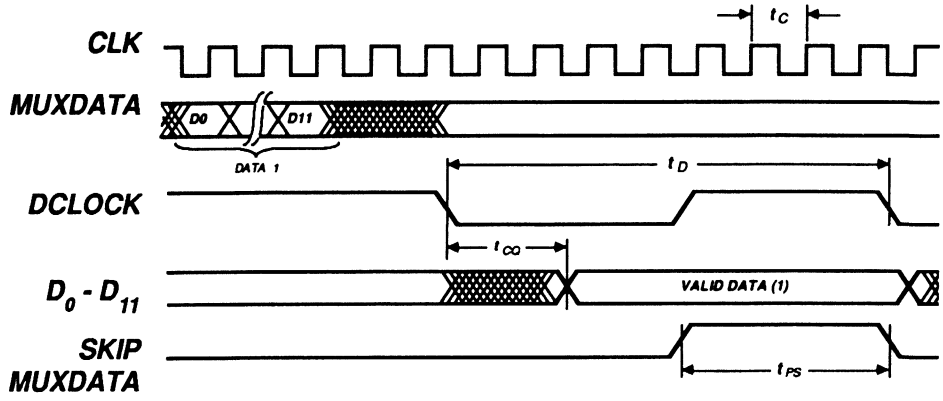
VS8001 12:1 Multiplexer Waveforms



VS8001 AC Characteristics: *(Over recommended operating conditions.)*

Parameter	Description	MIN	TYP	MAX	Units
t_C	CLK period	0.80	—	—	ns
t_D	DCLOCK period	9.6	—	—	ns
t_{SSU}	Set set-up time	2.0	—	—	ns
t_H	Set hold time	3.0	—	—	ns
t_{DSU}	Data set-up time	2.0	—	—	ns
t_{DH}	Data hold time	3.0	—	—	ns
t_{CMD}	Clock output (CLKOUT, NCLKOUT) to muxed data output (MUXDATA, NMUXDATA) timing	-50	—	+150	ps
jitter	CLK to MUXDATA, NMUXDATA (max-min), (HIGH to LOW) same part, same pin as constant conditions	—	<50	—	ps

VS8002 1:12 Demultiplexer Waveforms



VS8002 AC Characteristics:

(Over recommended operating conditions.)

Parameter	Description	MIN	TYP	MAX	Units
t_C	CLK period	0.80	—	—	ns
t_D	DCLOCK period	9.6	—	—	ns
t_{CQ}	Clock to Q data	0.5	—	2.5	ns
t_{PS}	Minimum pulse skip	3.0	—	—	ns
Phase Margin	MUXDATA phase timing margin with respect to CLK input	135	—	—	degrees

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{TT}) ..... -3.0 V to +0.5 V
Power Supply Voltage (V_{EE}) ..... V_{TT} + 0.7 V to -7.0 V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_c) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

Recommended Operating Conditions

ECL Power Supply Voltage (4), (V_{TT}) ..... -2.1 V to -1.9 V
Power Supply Voltage, (V_{EE}) ..... -5.46 V to -4.94 V
Operating Temperature Range (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

Notes: *(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*
(2) V_{TT} must be applied before any input signal voltage (V_{ECLIN}) and V_{ECLIN} must be greater than V_{TT} - 0.5 V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.
(4) When using internal ECL 100K reference level.

DC Characteristics

ECL Inputs/Outputs

(Over recommended operating conditions with internal V_{REF}. $V_{CC} = V_{CCA}$ = GND, Output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-600	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-50	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential ECL output pins must be terminated identically.

High Speed Inputs/Outputs

(V_{EE} = -5.2V , V_{CC} = GND, V_{TT} = -2.0V, T_C = 25°C. Input reference level (V_{REF}) = -3.5 V Typ.)
Complementary high speed output pins must be terminated equally.

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	—	-0.9	—	V	Output load: 50 Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	
ΔV_{OUT}	Output voltage swing	0.62	0.9	1.3	V	
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for all inputs

Notes: *1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.*
2) If a high speed input is used single-ended, a 100 pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed output pins must be terminated identically.
4) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.

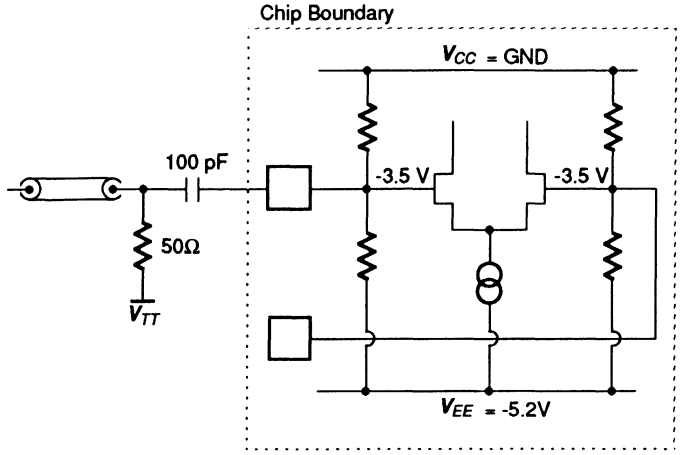
3

Power Dissipation: *(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)*

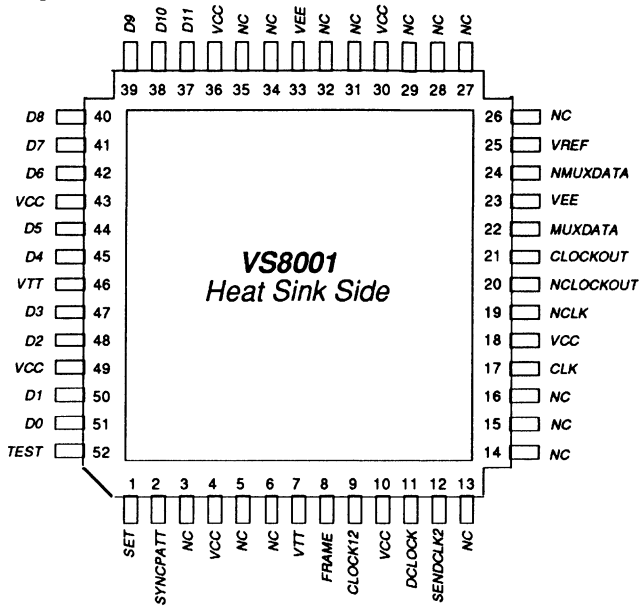
Parameter	Description	VS8001			VS8002			Units
		MIN	TYP	MAX	MIN	TYP	MAX	
I_{EE}	Power supply current from V_{EE}	—	415	520	—	435	550	mA
I_{TT}	Power supply current from V_{TT}	—	200	300	—	270	400	mA
P_D	Power dissipation	—	2.6	3.5	—	2.8	3.9	W

High Speed Inputs

High speed inputs (clock or data) are intended for single-ended AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs.



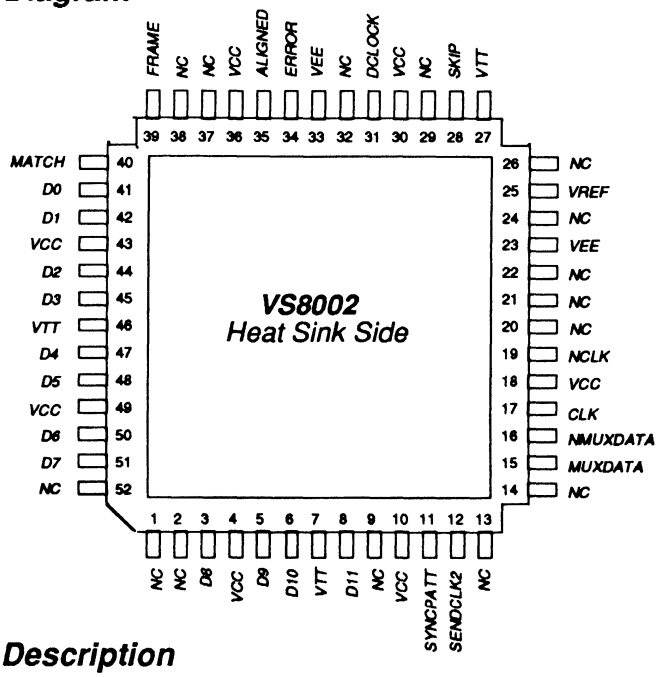
VS8001 Pin Diagram



VS8001 Pin Description

Pin #	Name	I/O	Description
17, 19	***CLK, NCLK***	I	High speed clock input (capacitively coupled)
21, 20	***CLOCKOUT, NCLOCKOUT***	O	High speed clock output
22, 24	***MUXDATA, NMUXDATA***	O	High speed serial data output
37-42, 44, 45, 47, 48, 50, 51	***D0-D11***	I	Parallel data inputs (ECL)
9	***CLOCK12***	O	Internally generated divide by 12 clock output (ECL)
11	***DCLOCK***	I	External divide by 12 clock input (ECL)
1	***SET***	I	Synchronization input (ECL)
52	***TEST***	I	Test hardware enable (ECL input). LOW for normal operation.
8	***FRAME***	O	Test pattern repeat confirmation (ECL output). Float or VCC for normal operation.
2	***SYNCPATT***	I	Test pattern alignment enable (ECL input). LOW for nornal operation.
12	***SENDCLOCK2***	I	"CLK2" pattern enable (ECL input). LOW for normal operation.
25	V_{REF}	I	ECL reference level input.
4, 10, 18, 30, 36, 43, 49	V_{CC}	I	Ground connection.
7, 46	V_{TT}	I	-2.0 V supply for internal reference generation & low power logic.
23, 33	V_{EE}	I	-5.2 V supply for high speed logic.
3, 5, 6, 13-16, 26-29, 31, 32, 34, 35	***NC***		No connection.

VS8002 Pin Diagram



VS8002 Pin Description

Pin #	Name	I/O	Description
17, 19	***CLK, NCLK***	I	High speed clock input (capacitively coupled)
15, 16	***MUXDATA, NMUXDATA***	I	High speed serial data input
41, 42, 44, 45, 47, 48, 50, 51, 3, 5, 6, 8	***DO-D11***	O	Parallel data outputs (ECL)
31	***DCLOCK***	I	Internally generated divide by 12 clock output (ECL)
28	***SKIP***	I	Causes one high speed serial bit to be skipped for word boundary shifting. A SKIP input causes data to become invalid for up to 3 DCLOCK periods. (ECL input)
35	***ALIGNED***	O	Indicates that the demux has found a match on three consecutive DCLOCK cycles (ECL output). Float or VCC for normal operation.
34	***ERROR***	O	Indicates that the internally generated pattern did not match the incoming data on at least one DCLOCK cycle since the error latch was reset (ECL output). Float or VCC for normal operation.
27	***TEST***	I	Test hardware enable (ECL input). LOW for normal operation.
39	***FRAME***	O	Test pattern repeat confirmation (ECL output). Float or VCC for normal operation.
40	***MATCH***	O	Indicates that the internally generated pattern matched he incoming demultiplexed data (ECL output). Float or VCC for normal operation.
11	***SYNCPATT***	I	Test pattern enable (ECL input). LOW for normal operation.
12	***SENDCLOCK2***	I	"CLK2" pattern enable (ECL input). LOW for normal operation.
25	V_{REF}	I	ECL reference level input.
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection.
7, 46	V_{TT}	I	-2.0 V supply for internal reference generation & low power logic.
23, 33	V_{EE}	I	-5.2 V supply for high speed logic.
1, 2, 9, 13, 14, 20-22, 24, 26, 29, 32, 27, 38, 52	***NC***		No connection.

Self-Test Feature

Test Description

The following is a description of the circuitry and method used to implement the self-test feature incorporated in the VS8001 and VS8002.

Because of the difficulty and cost associated with manually generating and detecting high speed data streams, the VS8001 and VS8002 have been designed with circuitry which enables the user to perform an at-speed functional evaluation of the parts in a system environment by using a single external stimulus: the high speed clock. The test circuitry, distributed between the two parts, consists of two pattern generators, control logic, and a twelve-bit comparator. The multiplexer generates a serial data pattern, and the demultiplexer detects the pattern and compares it for correctness.

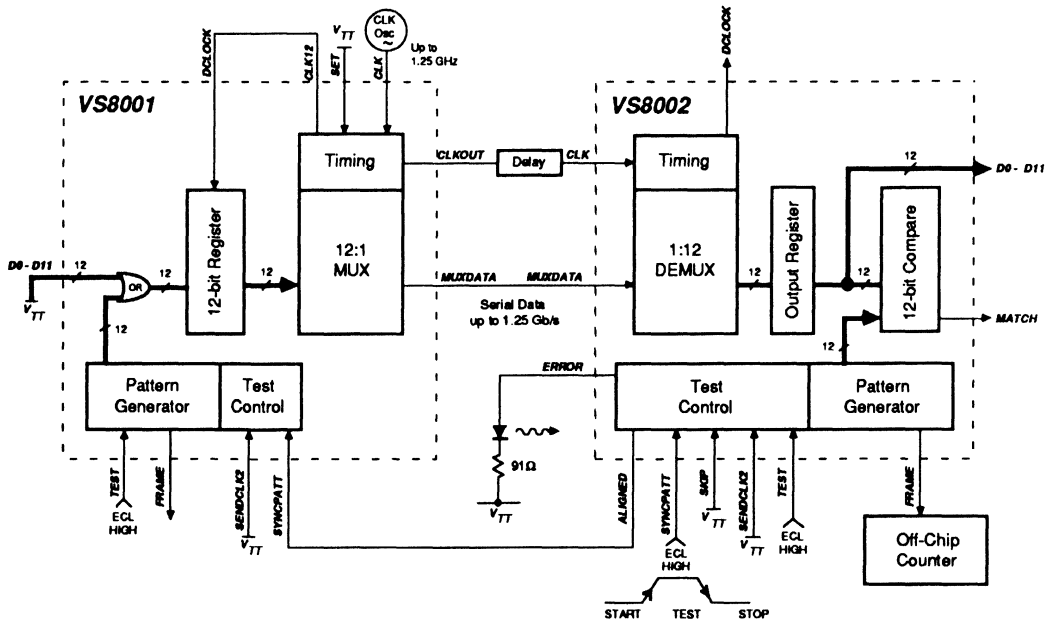
The pattern generator on the VS8001 creates twelve-bit patterns for the multiplexer, which then converts these twelve-bit words into a serial data stream. The serial output of the multiplexer is connected to the serial input of the demultiplexer. The demultiplexer converts this high speed serial data bit stream into twelve bit parallel data and compares the incoming data to patterns created by its own test pattern generator.

The pattern generators can make three different patterns: a synchronizing pattern (called *"SYNC"*), a transition pattern (called *"CLK2"*), and a pseudo-random pattern that repeats every 4095 words. The *SYNC* pattern is sent first to allow the demultiplexer to find word boundaries. During synchronization, the ***ALIGNED*** pin on the demultiplexer signals that the comparator has found a match on three successive words. This is followed by the *CLK2* pattern which signals the demultiplexer that the pattern is about to change to the 4095 word pseudo-random pattern. This allows the demultiplexer to start its pseudo-random pattern at the appropriate time to match the pattern being received on the incoming data stream from the multiplexer.

The incoming data pattern and the locally generated test pattern go to a twelve-bit comparator. The result of the comparison appears at the ***MATCH*** pin of the demultiplexer. A latch, which is reset upon entering the pseudo-random mode, detects any mismatch between the incoming data pattern and the locally generated test pattern. The latch state appears at the ***ERROR*** pin of the demultiplexer. On both parts, a one-period pulse on the ***FRAME*** pin signals that the pseudo-random pattern is repeating.

The test is controlled with the ***TEST*** and ***SYNCPATT*** pins on both parts. The diagram on the following page shows the self-test set-up in more detail.

Self-Test Set-Up



Test Hardware Blocks

VS8001:

The test hardware on the MUX consists of a 12-bit pattern generator with control logic. The individual blocks are described below.

Pattern Selector FSM

The pattern selector state machine selects the pattern generated by the MUX pattern generator. When ***SYNCPATT*** is LOW, the pattern selector state machine is reset and the pattern generator generates the *SYNC* pattern.

Pattern Generator

The pattern generator contains logic for static generation of two different 12-bit patterns and dynamic generation of a pseudo-random 12-bit pattern. The static patterns are the *"SYNC"* pattern (100101010110) and the *"CLK2"* pattern (101010101010). The pseudo-random pattern provides a pattern length of 4905 ***DCLOCK*** cycles. The first pattern in the sequence (001010101010) is explicitly detected. The result appears at the ***FRAME*** pin as a HIGH signal for one ***DCLOCK*** period out of every 4095 while in pseudo-random mode.

VS8002:

The test hardware on the DEMUX consists of a 12-bit pattern generator with control logic and a 12-bit comparator. The individual blocks are described briefly below.

Pattern Selector FSM

The pattern selector state machine selects the pattern generated by the DEMUX pattern generator. It also resets the error latch upon entering the pseudo-random test mode. When ***SYNCPATT*** is LOW, the pattern selector state machine is reset and the pattern generator generates the *SYNC* pattern.

Aligned FSM

When ***SYNCPATT*** is LOW and ***MATCH*** is HIGH for three consecutive ***DCLOCK*** cycles, the ***ALIGNED*** signal will go HIGH on the next cycle. This is called the "aligned" state. Once aligned the ***ALIGNED*** pin will stay HIGH until ***SYNCPATT*** goes LOW, forcing a reset of the aligned state machine. When aligned the DEMUX will not issue internally generated skip signals.

***ERROR* Latch**

The ***ERROR*** latch is set if ***TEST*** is HIGH and ***MATCH*** is LOW. It is reset when entering the aligned state or when the ***TEST*** pin is LOW. The purpose is to latch any mismatch detected during the pseudo-random test.

***SKIP* Edge Generator FSM**

If an internally generated skip is requested, this state machine translates the request to a rising edge and locks out internally generated skip signals for four ***DCLOCK*** cycles.

Pattern Generator

The pattern generator contains logic for static generation of two different 12-bit patterns and dynamic generation of a pseudo-random 12-bit pattern. The static patterns are the *"SYNC"* pattern (100101010110) and the *"CLK2"* pattern (101010101010). The pseudo-random pattern provides a pattern length of 4095 ***DCLOCK*** cycles. The first pattern in the sequence (001010101010) is explicitly detected. The result appears at the ***FRAME*** pin as a HIGH signal for one ***DCLOCK*** period out of each 4095 while in the pseudo-random mode.

Test Pins

VS8001:

There are 4 pins on the VS8001 which are used only for testing the part. The input pins used only for testing are ***TEST, SYNCPATT,*** and ***SENDCLK2.*** For normal operation, the ***TEST*** pin must be forced to ECL LOW or tied to V_{TT}. The one output pin used only for testing is ***FRAME.*** For normal operation, the termination of the ***FRAME*** pin is not critical. Usually, the output driver will be off. This pin may be properly terminated to V_{TT}, left floating, or tied to the V_{CC} supply. In test operations, all of the test pins should be properly terminated to V_{TT}.

***TEST* (ECL input pin)**

The input, ***TEST***, may be driven asynchronously. When ***TEST*** is LOW, all effects of the self-test hardware on the results of the MUX are asynchronously disabled. Explicitly, when the ***TEST*** pin is LOW, the output of the pattern generator is all zeros (000000000000).

When the ***TEST*** pin is HIGH and the high speed ***CLK*** and ***DCLOCK*** inputs are driven appropriately, the part is in *"test"* mode. In test mode, the self-test hardware is allowed to sequence and may effect the results on the output pins of the MUX chip. In test mode the 12 parallel data input pins must be driven to ECL LOW or tied to the V_{CC} power supply.

***SYNCPATT* (ECL input pin)**

The input pin, ***SYNCPATT,*** should be driven synchronously with respect to ***DCLOCK***. When ***SYNCPATT*** is LOW, the pattern selector state machine will be forced to the zero state. If in test mode and ***SYNCPATT***= LOW, the MUX pattern generator will generate the *"SYNC"* pattern (100101010110). This pattern will appear at the high speed serial output part of the MUX (left bit first). The DEMUX expects to receive this pattern for word boundary alignment.

When in test mode and ***SYNCPATT*** goes HIGH, the MUX pattern generator will change the pattern on the next ***DCLOCK*** cycle. The *CLK2* pattern (101010101010) will be generated for 3 ***DCLOCK*** periods to signal a change in test mode. The next ***DCLOCK*** cycle will start a pseudo-random pattern that repeats every 4095 ***DCLOCK*** cycles. In test mode, the pseudo-random pattern sequence continues until ***SYNCPATT*** goes LOW or ***SENDCLK2*** goes HIGH.

In the intended test flow, the ***ALIGNED*** signal from the DEMUX is used to drive the ***SYNCPATT*** input on the MUX chip. This allows the DEMUX to determine the time necessary for alignment using the *SYNC* pattern before the MUX changes to the pseudo-random test mode.

***SENDCLK2* (ECL input pin)**

The input pin, ***SENDCLK2,*** is provided to force the pattern generator to generate the ***CLK2*** pattern instead of the pseudo-random pattern. This feature is not intended for use within the typical test flow.

***FRAME* (ECL output pin)**

FRAME=HIGH indicates that the internally generated pattern (001010101010) was sent to the multiplexer's parallel data input register on the previous ***DCLOCK*** cycle. This pattern is the first word of the 4095 word pseudo-random

sequence. While in the pseudo-random mode, the ***FRAME*** pin has a HIGH signal for one ***DCLOCK*** period out of every 4095.

VS8002:

There are some pins on the VS8002 which are used only for testing the part. The input pins used only for testing are ***TEST, SYNCPATT,*** and ***SENDCLK2.*** For normal operation, the ***TEST*** pin must be forced to ECL LOW or tied to the V_{TT} supply. For normal operation, ***SYNCPATT*** and ***SENDCLK2*** may be left floating, forced to ECL LOW, or tied to the V_{TT} supply. The output pins used only for testing are ***MATCH, ALIGNED, ERROR,*** and ***FRAME.*** For normal operation, the termination of these output pins is not critical. Usually, the output drivers will be off. These pins may be properly terminated to V_{TT}, left floating, or tied to the V_{CC} supply. In test operations, all of the test pins should be properly terminated to V_{TT}.

TEST **(ECL Input pin)**

The input pin, ***TEST,*** may be driven asynchro-nously. When ***TEST*** is LOW, all effects of the self-test hardware on the results of the DEMUX are asynchronously disabled. Explicitly, when the ***TEST*** pin is LOW, no ***SKIPs*** (word rotation) will be internally generated and the error latch input will be forced LOW.

When the ***TEST*** pin is HIGH and the high speed ***CLK*** inputs are driven appropriately, the part is in *"test"* mode. In test mode, the self-test hardware is allowed to sequence and may effect the results on the output pins of the DEMUX chip.

SYNCPATT

The input pin, ***SYNCPATT,*** should be driven synchronously with respect to ***DCLOCK.*** When ***SYNCPATT*** is LOW, the pattern selector, word alignment selector, and ***SKIP*** edge generator state machines will all be forced to their zero states. In this state, the DEMUX pattern generator will generate the *SYNC* pattern (100101010110). This allows external word alignment using the ***MATCH*** output pin and the ***SKIP*** input pin.

When in test mode and ***SYNCPATT*** goes HIGH, the DEMUX pattern generator will continue to generate the *SYNC* pattern until certain conditions are met. If the generated pattern matches the demultiplexed input data, then ***MATCH*** will go HIGH. If no match is detected, then the DEMUX will issue itself a ***SKIP*** signal (through the ***SKIP*** edge generator state machine). After a ***SKIP*** has been issued in this manner, the ***MATCH*** signal will be ignored for four ***DCLOCK*** cycles so that transient data during word boundary rotation cannot cause an unintended ***SKIP*** to occur. In this state, the DEMUX will react normally to externally driven ***SKIP*** signals, so the ***SKIP*** pin should be held LOW for this test. Then, the DEMUX will issue ***SKIP*** signals until ***MATCH*** is HIGH for three consecutive ***DCLOCK*** cycles. On the following ***DCLOCK*** cycle the ***ALIGNED*** signal will go HIGH. Call this the *"aligned"* state. Once aligned, the DEMUX will not issue internally generated ***SKIP*** signals unless the aligned state machine is reset by cycling the ***SYNCPATT*** input.

The expected test sequence is that the *SYNC* pattern will be received until the DEMUX is aligned. Then a *CLK* divide-by-2 pattern (101010101010) will be received for 3 ***DCLOCK*** cycles to signal a change in test mode. The next ***DCLOCK*** cycle will start a pseudo-random pattern that repeats every 4095 ***DCLOCK*** cycles. The DEMUX pattern selector state machine looks for ***ALIGNED*** to be HIGH and ***MATCH*** to be LOW. This signals a change in test pattern on the input data stream. Notice the ***CLK2*** pattern is not specifically detected, only a mis-match. Thus, once aligned, an error in detecting the *SYNC* pattern will put the DEMUX in pseudo-random test mode.

SENDCLK2 **(ECL Input pin)**

The input pin, ***SENDCLK2,*** is provided to force the pattern generator to generate the ***CLK2*** pattern instead of the pseudo-random pattern. This feature is not intended for use within the typical test flow.

MATCH **(ECL output pin)**

The ***MATCH*** pin is the registered output of the 12-bit comparator. ***MATCH*** = HIGH indicates that the internally generated pattern matched the incoming demultiplexed data on the previous ***DCLOCK*** cycle.

***ALIGNED* (ECL output pin)**

ALIGNED= HIGH indicates that the DEMUX has found a match on three consecutive ***DCLOCK*** cycles. When ***ALIGNED*** first goes HIGH the DEMUX is ready to transition to the pseudo-random pattern mode. In the intended test flow ***ALIGNED*** is used to drive the ***SYNCPATT*** input on the MUX chip.

***ERROR* (ECL output pin)**

ERROR= HIGH indicates that the internally generated pattern did not match the incoming demultiplexed data on at least one ***DCLOCK*** cycle since the ***ERROR*** latch was reset.

***FRAME* (ECL output pin)**

FRAME= HIGH indicates that the internally generated pattern (001010101010) was sent to the 12-bit comparator on the previous ***DCLOCK*** cycle. This pattern is the first word of the 4095 word pseudo-random sequence. While in the pseudo-random mode, the ***FRAME*** pin has a HIGH signal for one ***DCLOCK*** period out of every 4095.

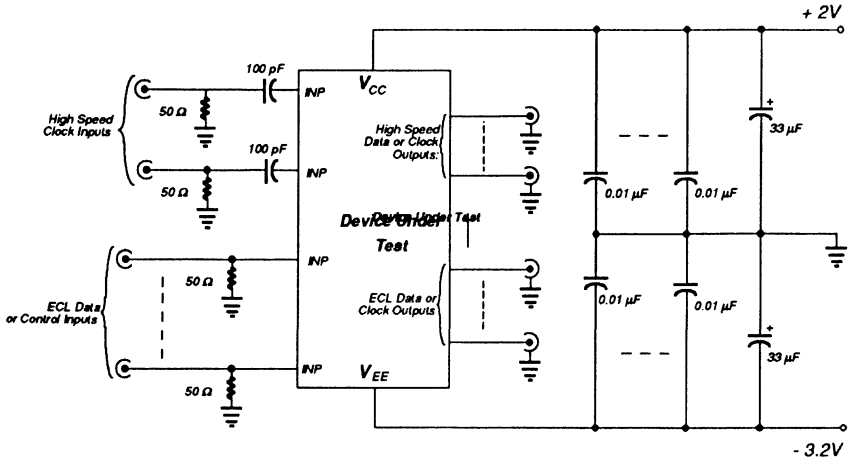
VS8001/VS8002 DUT Boards

The VS8001DUT and VS8002DUT are circuit boards which provide a test bed suitable for evaluating the performance characteristics of the VS8001 12:1 Multiplexer and the VS8002 1:12 Demultiplexer in 52 pin leadless chip carriers (LCC).

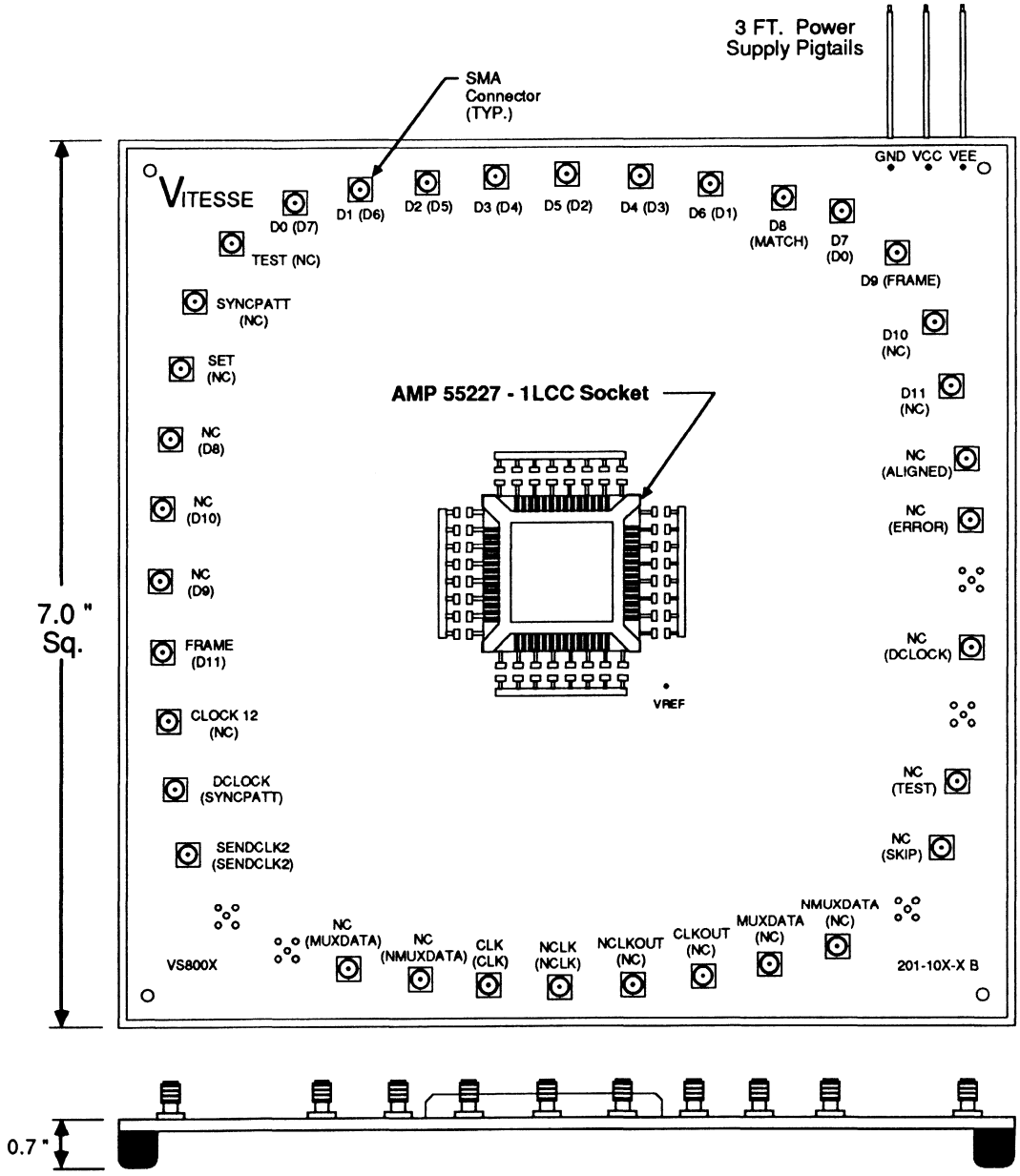
A schematic of the evaluation board is shown below. This board provides controlled impedance transmission for all signal lines and decoupling for the power supplies. The signal traces have a characteristic impedance of 50 Ω. All ECL input lines are terminated with 50 Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 100 pF blocking capacitors. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated with 50 Ω in the measuring instrument.

Normally, the VS8001 and VS8002 operate in an ECL environment with standard ECL power forms (Ø V, -2.0 V, and -5.2 V). In order to simplify interface to standard ground referenced test equipment, however, the circuit board power forms are offset so that the shield con-nectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power form.

The device socket is an AMP 55227-1LCC socket and was chosen for minimum inductance and shortest possible stub length. The figures on the next page show the physical dimensions as well as the names of the connectors on the evaluation boards.



VS8001/VS8002 DUT Boards



Notes: 1) This drawing represents both the VS8001 and VS8002 configurations. (Connection labels given in parentheses are for the VS8002.)

2) NC = No connection.

VS8004/VS8005

4:1 Multiplexer - 1:4 Demultiplexer Chip Set (2.5 Gb/s)

Features

- Superior performance: serial data up to 2.5 Gb/s
- ECL 100K/10KH compatible parallel data inputs/outputs
- Single ECL power supply: V_{EE} = -5.2 V ± 0.26 V
- Available in commercial or industrial temperature ranges
- Proven E/D mode GaAs technology
- Differential or single-ended inputs and outputs
- Low Power Dissipation 1.5 to 1.6 Watts (Typ)
- 28-pin leaded or leadless ceramic chip carrier

Functional Description

Introduction

The VS8004 and VS8005 are data conversion devices capable of serial data rates up to 2.5 Gb/s, transforming 4-bit wide parallel data to serial data and serial data to 4-bit wide parallel data.

The VS8004/VS8005 are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 28-pin leaded or leadless chip carrier. Refer to Section 6, "Packaging" for a complete description of this package.

VS8004

The VS8004 is an ultra high speed 4 bit parallel to serial data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The parallel inputs ***[D(0:3), ND(0:3)]*** accept data at rates up to 625 Mb/s. The differential serial data output ***(SDATA, NSDATA)*** presents the data sequentially from the parallel data inputs at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input ***(CLK, NCLK)***. An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output ***(CLK4, NCLK4)***. This clock signal is provided so that incoming parallel signals can be synchronized to arrive at the input data registers simultaneously. An internal bias network is provided at all inputs to simplify capacitive coupling.

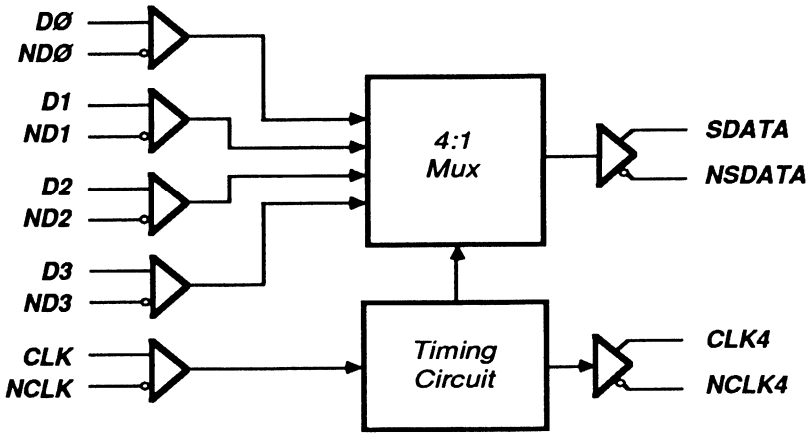
VS8005

The VS8005 is an ultra high speed 4-bit parallel to serial data converter suitable for digital voice or data communications applications. All inputs and outputs can be used differentially or single-ended. The differential serial data inputs ***(SDATA, NSDATA)***accept data at rates up to 2.5 Gb/s, synchronous with the differential high speed clock input ***(CLK, NCLK)***. The parallel outputs ***[D(0:3), ND(0:3)]*** present the data sequentially at rates up to 625 Mb/s. An internal timing generator receives the high speed clock input and divides it by four to create a differential clock output ***(CLK4, NCLK4)*** which is synchronous with the parallel data outputs. A control input ***(SKIP, NSKIP)*** is provided to allow realignment of the output parallel word boundaries.

Applications

- High speed instrumentation and test equipment
- Fiber-optic communication
- Local area networks
- Serialization of computer backplanes
- Computer to computer interfaces s
- Serial control buses for aerospace environments

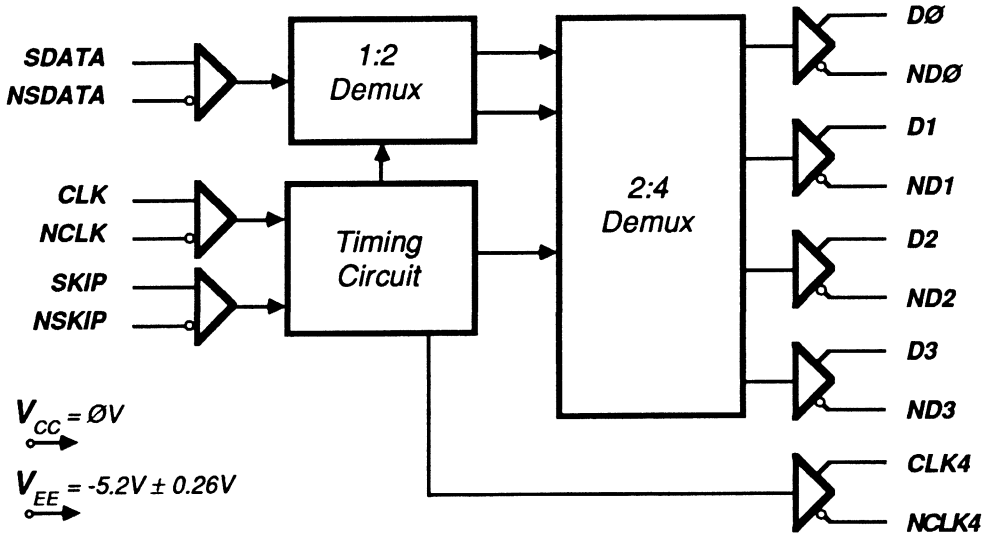
VS8004 Block Diagram



V_{CC} = ØV

V_{EE} = -5.2V ± 0.26V

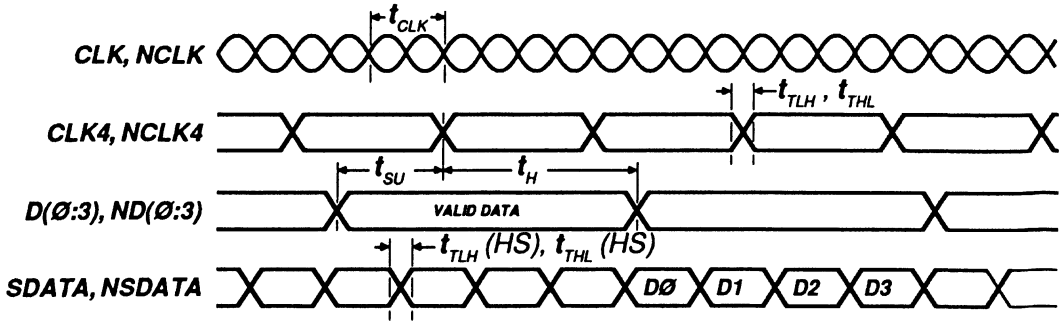
VS8005 Block Diagram



V_{CC} = ØV

V_{EE} = -5.2V ± 0.26V

VS8004 Waveforms

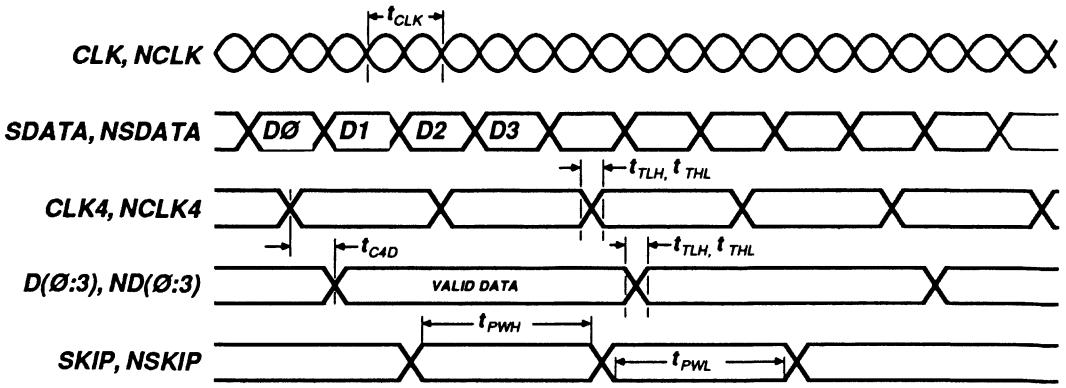


VS8004 AC Characteristics:

(Over recommend operating conditions.)

Parameter	Description	MIN	TYP	MAX	Units
t_{CLK}	High speed clock period	400	—	—	ps
t_{SU}	D(Ø:3), ND(Ø:3), set-up time with respect to CLK4, NCLK4	900	—	—	ps
t_H	D(Ø:3), ND(Ø:3), hold time with respect to CLK4, NCLK4	-300	—	—	ps
t_{TLH}(HS), t_{THL}(HS)	SDATA, NSDATA transition time (LO to HI, HI to LO) while driving 50Ω to -2.0V	—	150	—	ps
jitter	CLK, NCLK to SDATA, NSDATA (max-min), (HI to LO), same part, same pin at constant conditions	—	<50	—	ps
t_{TLH}, t_{THL}	ECL output transition time (LO to HI, HI to LO) while driving 50Ω (CLK4, NCLK4, D(0:3), ND(0:3)) to -2.0V	—	500	—	ps

VS8005 Waveforms



VS8005 AC Characteristics:

(Over recommended operating conditions.)

Parameter	Description	MIN	TYP	MAX	Units
t_{CLK}	High speed clock period (CLK, NCLK)	400	—	—	ps
t_{C4D}	CLK4, NCLK4 to D(0:3), ND(0:3)	—	400	—	ps
t_{PWH}	SKIP, NSKIP pulse width (HIGH)	2	—	—	ns
t_{PWL}	SKIP, NSKIP pulse width (LOW)	2	—	—	ns
t_{TLH} t_{THL}	ECL output transition time (LOW to HIGH, & HIGH to LOW) for D(0:3), ND(0:3), and CLK4, NCLK4 (Driving 50Ω)	—	500	—	ps
phase margin	SDATA, NSDATA phase timing margin with respect to CLK, NCLK (@ 2.5GHz)	135	—	—	degrees

Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{EE}) ..... V_{CC} (GND) to - 6.0 V
ECL Input Voltage Applied, (V_{ECLIN}) (2) ..... -2.5 V to 0.5 V
High Speed Input Voltage Applied, (V_{HSIN}) (3) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current (output HIGH), (I_{OUT}) ..... -50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

Recommended Operating Conditions

Power Supply Voltage, (V_{EE}) ..... -5.46 V to -4.94V
Operating Temperature Range, (T) (4) ..... (Commercial) 0° to +70°C, (Industrial) -40° to +85°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without causing permanent damage, but are stress ratings only. Functionality at or above the values listed is not implied, and exposure to these values for extended periods may affect device reliability.

(2) V_{EE} must be applied before any input signal voltage (V_{ECLIN}).

(3) Internally biased to -3.5 V for AC coupling.

(4) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC Characteristics

High Speed Inputs:

(Over recommended operating conditions with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V)

Parameter	Description	MIN	TYP	MAX	Units	Conditions
V_{IH}	Input HIGH Voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal
V_{IL}	Input LOW Voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal
V_{REF}	Reference Level	—	-3.5	—	V	—

Notes: 1) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.

2) A reference generator is built in to each high speed input, and these inputs are intended to be AC coupled.

3) If a high speed input is used single-ended, a 100 pF capacitor must be connected between the unused high speed or complement input and the power supply (V_{EE}).

DC Characteristics *(Continued)*

High Speed Outputs: *(Over recommended operating conditions. V_{CC} = GND, output load = 50Ω to -2.0V)*

Parameter	Description	MIN	TYP	MAX	Units	Conditions
V_{OH}	Output HIGH Voltage	-0.8	-0.5	-0.3	V	Terminated to -2.0 V through 50 Ω
V_{OL}	Output LOW Voltage	-2.0	-1.8	-1.6	V	Terminated to -2.0 V through 50 Ω

Notes: Differential high speed output pairs must be terminated identically

ECL Inputs and Outputs: *(Over recommended operating conditions with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V)*

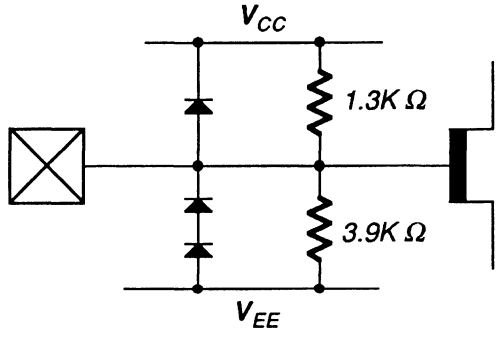
Parameter	Description	MIN	TYP	MAX	Units	Conditions
V_{OH}	Output HIGH Voltage	-1020	—	-600	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW Voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH Voltage	-1040	—	-600	mV	Guaranteed HIGH for ECL inputs
V_{IL}	Input LOW Voltage	-2000	—	-1600	mV	Guaranteed LOW for ECL inputs
I_{IH}	Input HIGH Current	—	500	1000	µA	$V_{IN} = V_{IH}$ (max)
I_{IL}	Input LOW Current	-1000	-500	—	µA	$V_{IN} = V_{IL}$ (min)

Notes: 1) Differential ECL output pairs must be terminated identically.
2) Leakage currents exceed ECL specifications due to the internal bias network which is connected to all inputs.

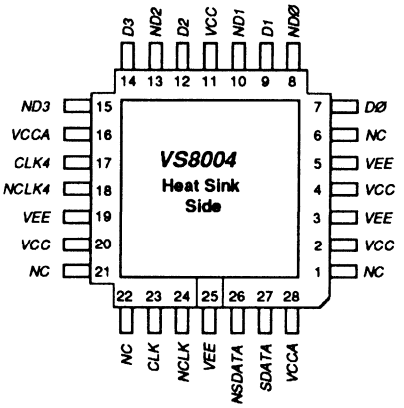
Power Dissipation: *(Over recommended operating conditions. V_{CC} = GND, outputs open circuit)*

Parameter	Description	VS8004			VS8005			Units
		MIN	TYP	MAX	MIN	TYP	MAX	Units
I_{EE}	Power supply current (V_{EE})	—	270	350	—	310	400	mA
P_D	Power dissipation	—	1.5	1.9	—	1.6	2.2	W

ECL Input Equivalent Circuit



VS8004 Pin Diagram



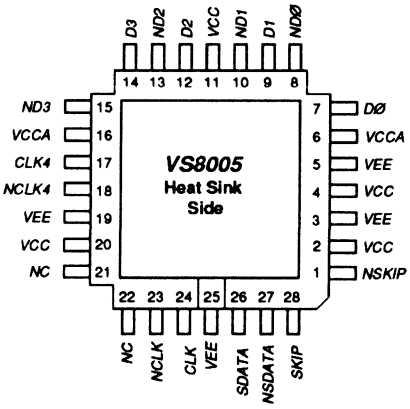
VS8004 Pin Description

Pin #	Name	I/O	Description
23, 24	CLK, NCLK	I	Differential high speed clock inputs
27, 26	SDATA, NSDATA	O	Differential high speed serial data outputs
17, 18	CLK4, NCLK4	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	D(Ø:3), ND(Ø:3)	I	Differential parallel data inputs (ECL)
3, 5, 19, 25	V_{EE}		-5.2 V supply voltage
2, 4, 11, 20	V_{CC}		Ø V ground connection
16, 28	V_{CCA}		Ø V output ground connection
1, 6, 21, 22	NC		No connection

NOTES:

1) *The heat sink is connected to V_{EE} (pin 25). To prevent a short circuit between V_{CC}, V_{CCA} (Ø V normally) and V_{EE} (-5.2 V normally), do not connect this heat sink to ground. (Ø V).*
2) *The leadless version pin-out is the same as the leaded.*

VS8005 Pin Diagram



VS8005 Pin Description

Pin #	Name	I/O	Description
24, 23	CLK, NCLK	I	Differential high speed clock inputs
26, 27	SDATA, NSDATA	I	Differential high speed serial data inputs
17, 18	CLK4, NCLK4	O	Differential divide by 4 clock outputs (ECL)
7-10, 12-15	D(Ø:3), ND(Ø:3)	I	Differential parallel data inputs (ECL)
28, 1	SKIP, NSKIP	I	Differential word boundary inputs (ECL)
3, 5, 19, 25	V_{EE}		-5.2 V supply voltage
2, 4, 11, 20	V_{CC}		Ø V ground connection
6, 16	V_{CCA}		Ø V output ground connection
21, 22	NC		No connection.

NOTES:

1) *The heat sink is connected to V_{EE} (pin 25). To prevent a short circuit between V_{CC}, V_{CCA} (Ø V normally) and V_{EE} (-5.2 V normally), do not connect this heat sink to ground.*
2) *The falling edge of SKIP causes realignment of the parllel word boundary making parallel data invalid for three CLK4, NCLK4 (12 CLK, NCLK) periods.*
3) *The leadless version pinout is the same as the leaded.*

VS8004/VS8005 DUT Boards

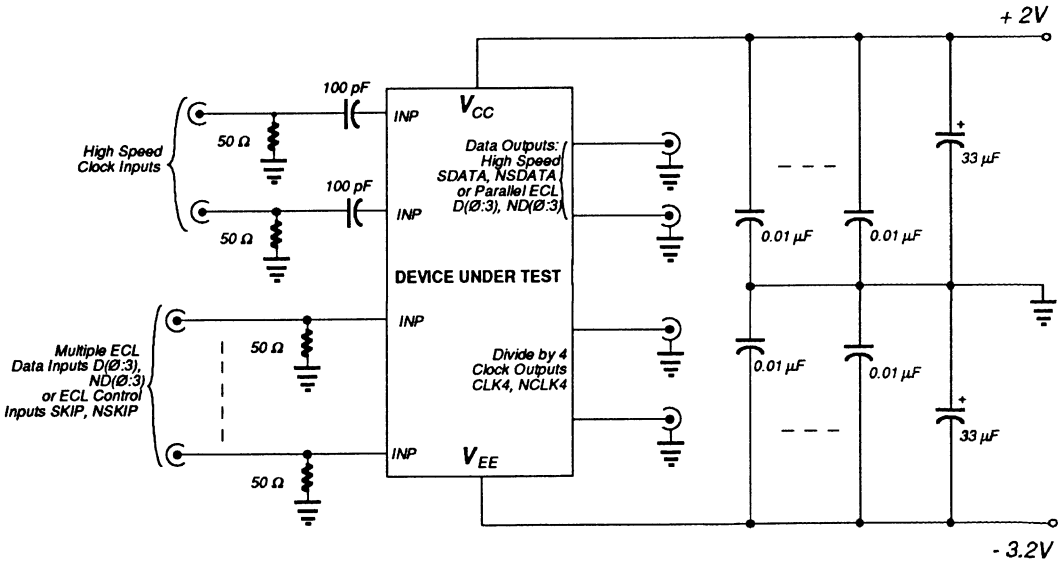
The VS8004FDUT/VS8005FDUT evaluation boards are special purpose circuit boards which provide a test bed suitable for evaluating the high performance characteristics of the VS8004 4:1 Multiplexer or the VS8005 1:4 Demultiplexer in the 28 pin leaded ceramic chip carrier.

The figure below is a schematic representation of these circuit boards. These boards provide a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50Ω. All ECL input lines are terminated with 50Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 100 pF blocking capacitors. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument.

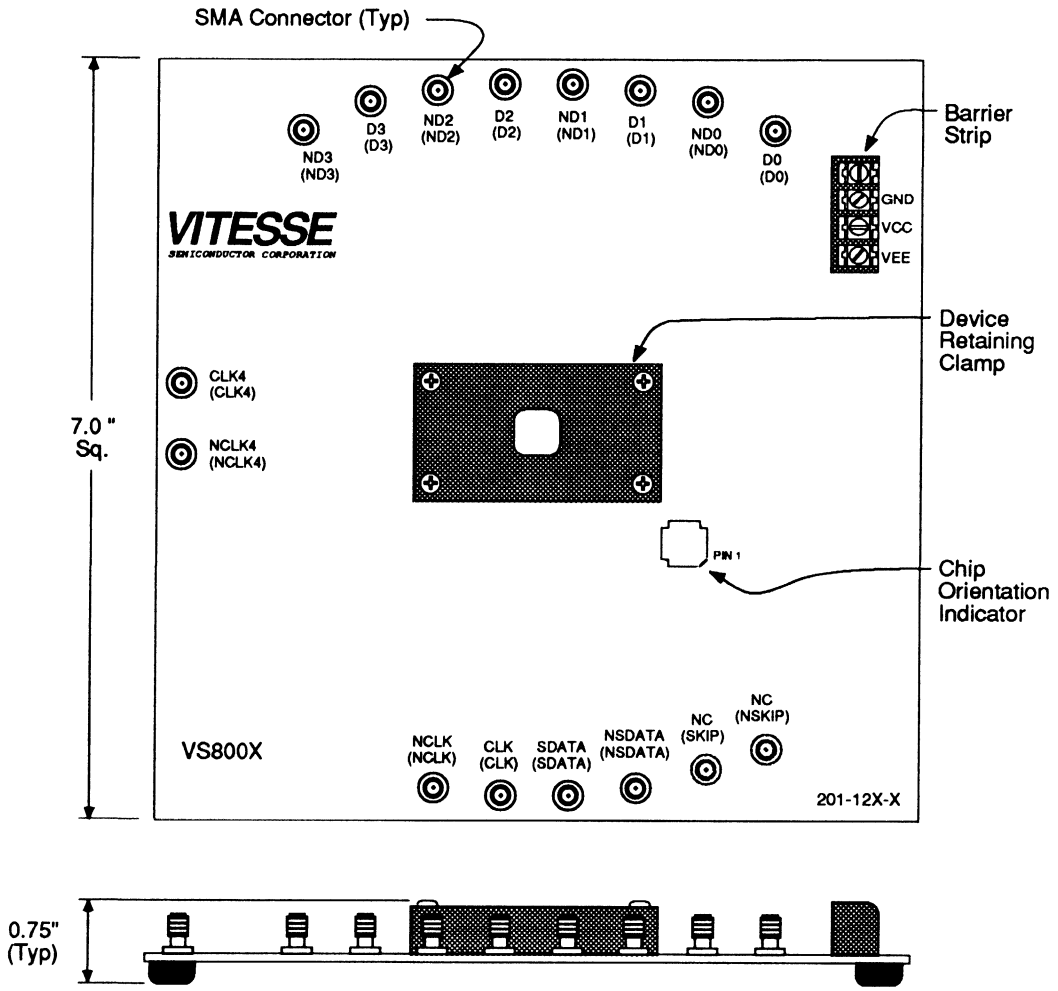
Normally, the VS8004 and VS8005 operate in an ECL environment with standard ECL power forms: ØV and -5.2V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power forms are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power form.

The device to be tested is held in place with a pressure retaining fixture. The figure on the following page shows the physical dimensions and the connection labels for the evaluation boards.

VS8004/VS8005 DUT Board Schematics



VS8004/VS8005 DUT Boards



Notes: 1) This drawing represents both the VS8004FDUT and VS8005FDUT configurations. (Connection labels given in parentheses are for the VS8005.)

2) NC = No connection. NOTE: These connectors are omitted on the VS8004FDUT version of this evaluation board.

VS8010 Series

SONET - High Speed 8 Bit Mux/Demux Products

Features

- Serial data: up to 1.25 Gb/s
- ECL 100K/10KH compatible parallel data inputs/outputs
- Standard ECL power supplies: V_{EE} = -5.2 v ± 0.26 V, V_{TT} = -2.0 V ± 0.1 V
- VS8010: 8 bit Mux/Demux and SONET frame detection and recovery
- VS8011: 8 bit Mux
- VS8012: 8 bit Demux and SONET frame detection and recovery
- Compatible with STS-3 to STS-24 SONET applications

Functional Description

Introduction

The VS8010, VS8011 and VS8012 are high speed SONET compatible 8-bit data conversion devices capable of serial data rates up to 1.25 Gb/s. The VS8010 series can be used for STS-3 through STS-24 SONET applications.

The VS8010 Series are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leaded or leadless chip carrier. Refer to Section 6, "Packaging" for a complete description of this package.

VS8010

The VS8010 integrates an 8:1 multiplexer, 1:8 demultiplexer, and SONET frame detection and recovery circuitry all on one chip.

8:1 Multiplexer Circuit

The 8:1 multiplexer accepts 8 parallel ECL data inputs ***[D(1:8)]*** at rates up to 155 Mb/s and multiplexes them into a single bit stream at speeds up to 1.25 Gb/s. The parallel data inputs are clocked into the input registers with ***BYCLK***, an ECL input operating at up to 155 MHz. The high speed clock input ***(CLKI)*** is divided by 8 ***(CLK8)*** and used to synchronize the parallel data to the timing generator. ***CLK8*** then loads the parallel data into the buffer registers. An on-chip circuit detects internal set up and hold violations caused by improperly related ***BYCLK*** and ***CLK8*** falling edges. An external signal ***(SYNC)*** may be used to correct ***CLK8*** phase by 180°. If a set-up or hold violation has been detected, a ***SYNC*** input causes ***CLK8*** to be inverted on the next ***BYCLK*** falling edge, thereby guaranteeing a safe ***CLK8*** and ***BYCLK*** relationship. If no set-up and hold violation has been detected ***SYNC*** has no impact on the circuit.

The high speed differential clock input is brought on-chip at ***CLKI, CLKIN***. The high speed differential serial data is provided at the ***DO, DON*** outputs. The high speed differential clock signal is transmitted off chip via the high speed outputs ***CO, CON***.

1:8 Demultiplexer Circuit

The 1:8 demultiplexer converts serial data at up to 1.25 Gb/s into an 8-bit parallel data stream at up to 155 Mb/s. The high speed differential serial input is at ***DI, DIN***. Valid parallel data outputs are indicated by the divide by 8 clock output ***BYCKO***. The demultiplexer also contains SONET frame detection and recovery circuitry.

Frame Recovery Circuit

The frame recovery circuits are enabled by a falling edge on the ***OOFN*** input. Once enabled, the frame recovery circuits start looking for the SONET framing sequence. Once the frame is detected, a confirmation signal is sent off-chip through the low power ECL output ***FP***. The frame detection confirmation signal also disables the frame recovery circuits.

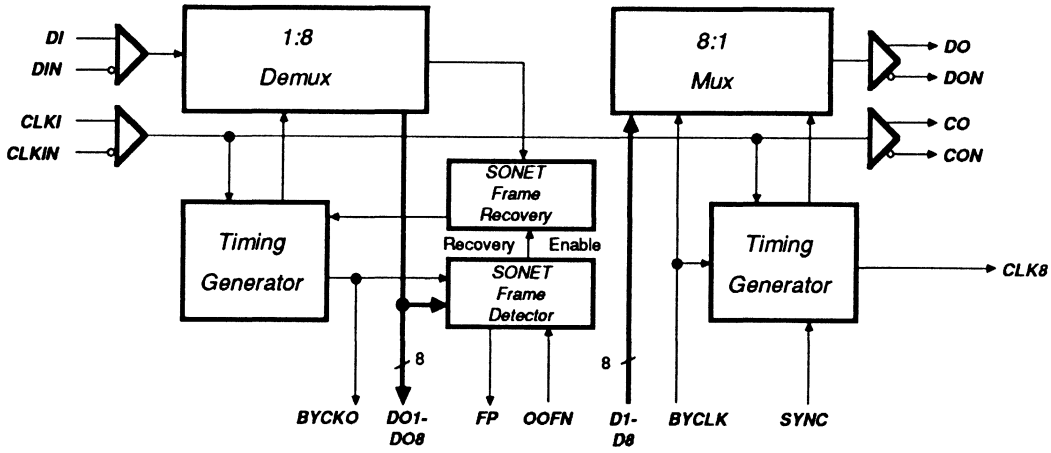
VS8011

The VS8011 is a high speed 8:1 multiplexer. The operation of the VS8011 exactly parallels that of the VS8010 8:1 Multiplexer circuitry described previously.

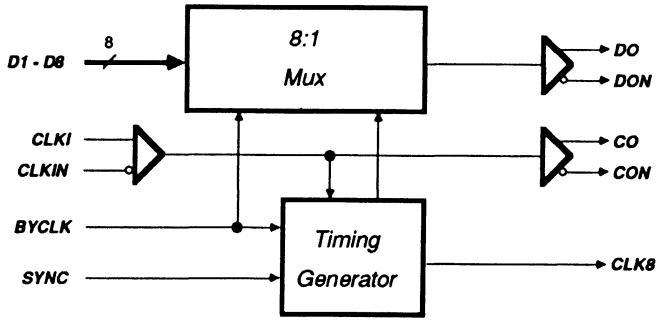
VS8012

The VS8012 integrates a 1:8 Demux and SONET frame recovery and detection circuitry on one chip. The operation of the VS8012 exactly parallels that of the VS8010 1:8 Demultiplexer and Frame Recovery circuits with the following exception. The frame recovery circuits are enabled by a falling edge on the ***OOFN*** ECL input when the additional ***FDIS*** ECL input is low. When the ***FDIS*** input is high the falling edge of ***OOFN*** disables the frame recovery circuit. The ***FDIS*** input is included to provide an alternative means of disabling the frame recovery circuit during device evaluation. In normal operation this input is wired to V_{TT} and the frame recovery circuit is disabled when serial F1's and F2's appear at the high speed differential serial data input ***(DI, DIN)***.

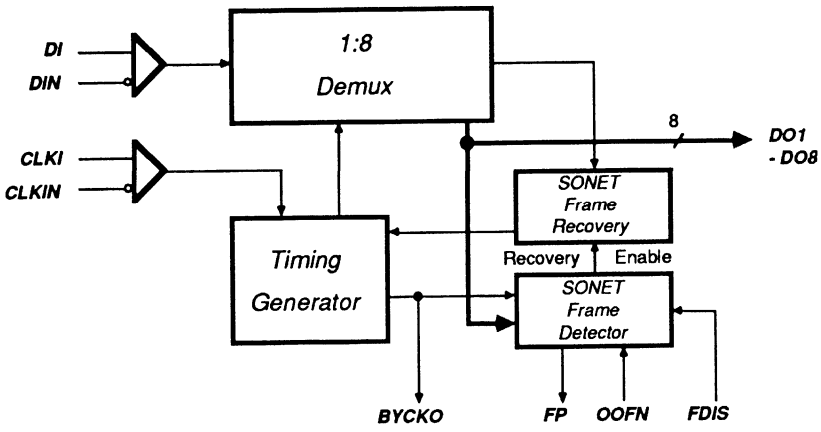
VS8010 Block Diagram



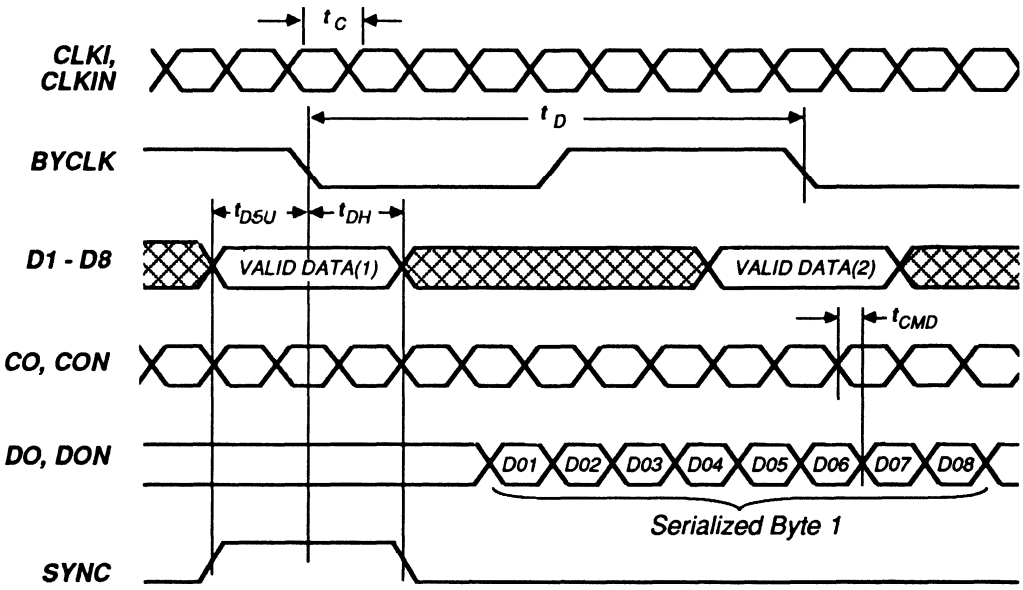
VS8011 Block Diagram



VS8012 Block Diagram



Multiplexer Waveforms (VS8010, VS8011)



Notes:

= *Don't care*

8 x clock period of CLKI = BYCLK period

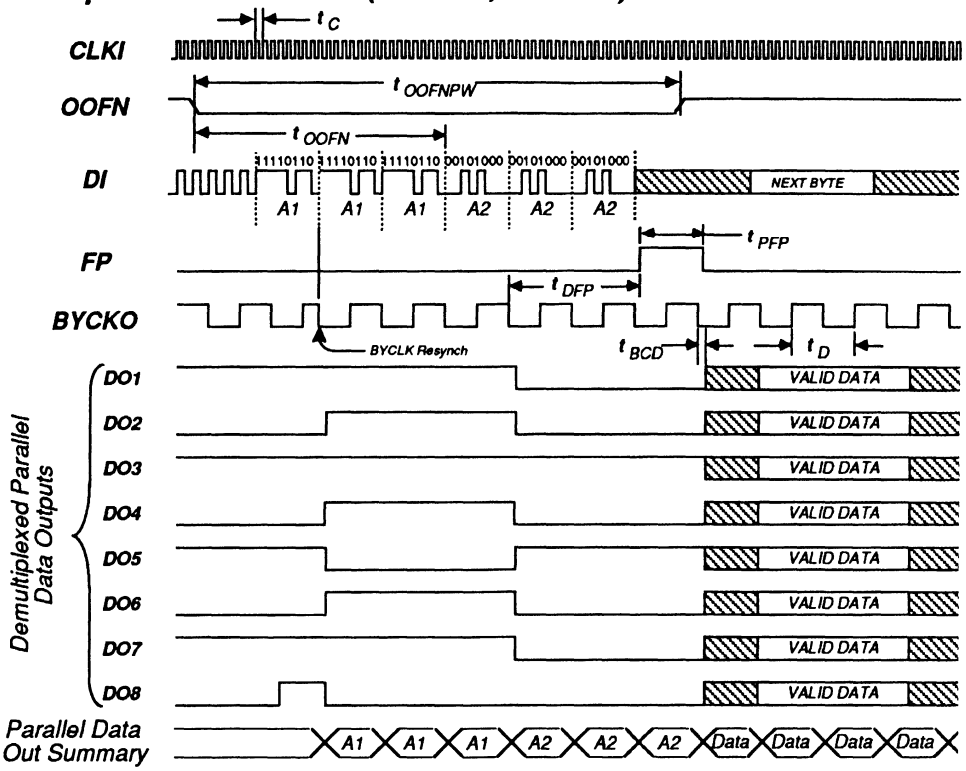
Multiplexer AC Characteristics (VS8010, VS8011):

(Over recommended operating conditions.)

Parameter	Description	MIN	TYP	MAX	Units
t_C	Clock period *	0.8	—	—	ns
t_D	BYTE clock period	6.4	—	—	ns
t_{DSU}	Parallel data set-up time	2.0	—	—	ns
t_{DH}	Data hold time	1.0	—	—	ns
t_{CMD}	High speed clock output (CO, CON) to muxed data output (DO, DON) timing	—	500	—	ps
jitter	CLKI, CLKIN to DO, DON (max-min, (HIGH to LOW), same part, same pin at constant conditions	—	50	—	ps

* The parts are guaranteed to operate from DC to a maximum frequency of 1.25 GHz.

Demultiplexer Waveforms (VS8010, VS8012)



Note: The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above utilize an STS-3 framing sequence for convenience. Thus, in this example, valid data is output after the third A2 in the SONET framing sequence.

Demultiplexer AC Characteristics (VS8010, VS8012):

(Over recommended operating conditions.)

Parameter	Description	MIN	TYP	MAX	Units
t_C	Clock period *	0.8	—	—	ns
t_D	BYTE clock period ($t_D = t_C \times 8$)	6.4	—	—	ns
t_{DFP}	FP rising edge from parallel data output change from F1 to F2 ($t_{DFP} = t_D \times 2$)	—	12.8	—	ns
t_{PFP}	FP pulse width ($t_{PFP} = t_D$)	6.4	—	—	ns
t_{OOFN}	OOFN falling edge before A1 changes to A2 ($t_{OOFN} = t_D \times 4$)	—	25.6	—	ns
t_{OOFNPW}	OOFN pulse width ($t_{OOFNPW} = t_D$)	6.4	—	—	ns
phase margin	Serial data phase timing margin with respect to high speed clock	135	—	—	degrees
t_{BCD}	Falling edge of **BYCKO** to valid parallel data output	t_c	t_c+0.5	t_c+1.5	ns

* If t_C changes, all the remaining parameters change as indicated by the equations.

SONET Frame Recovery and Detection (VS8010, VS8012)

Circuit Operation

The frame recovery circuits are enabled on the falling edge of the ***OOFN*** ECL input. Once enabled, the frame recovery circuit looks for the SONET framing sequence.

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000) The first serial bit starts at the left of the byte. The table below shows the number of A1 and A2 bytes in each SONET frame for different line rates.

STS LEVEL	*LINE RATE (Mb/S)*	*# OF A1 BYTES*	*# OF A2 BYTES*
STS-3	*155.520*	*3*	*3*
STS-9	*466.560*	*9*	*9*
STS-12	*622.080*	*12*	*12*
STS-18	*933.120*	*18*	*18*
STS-24	*1244.16*	*24*	*24*
STS-48	*2488.32*	*48*	*48*

Example. STS-24 has 24 A1s and 24 A2s:

$A1_1A1_2A1_3$.....$A1_{24}A2_1A2_2A2_3$.....$A2_{24}$

The VS8010 Series SONET recovery circuits operate from STS-3 to STS-24. The frame re-covery circuits look for 3 A1s followed by 3 A2s. The byte clock out ***(BYCKO)*** and parallel byte data out ***(DO_1-DO_8)*** become invalid on the falling edge of ***OOFN*** and become valid when A1 changes to A2. The frame recovery circuits align the received serial data on byte boundaries for demultiplexing by controlling the timing generator. The byte boundary alignment is based on specific A1 and A2 byte recognition.

The VS8010/12 have been designed to recognize 3 A1s followed by 3 A2s, and therefore recognize frames and align on byte boundaries for STS-3 through STS-24 line rates. As shown below, the framing sequence always contains 3 A1s followed by 3 A2s.

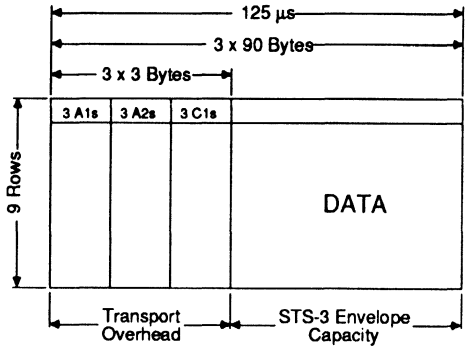
STS-24	(24 A1s & 24 A2s)
STS-18	(18 A1s & 18 A2s)
STS-12	(12 A1s &12 A2s)
STS-9	(9 A1s & 9 A2s)
STS-3	(3 A1s & 3 A2s)

The falling edge of ***OOFN*** must occur at least 4 byte clock periods before A1 changes to A2. The pulse width of ***OOFN*** must be at least 1 byte clock period.

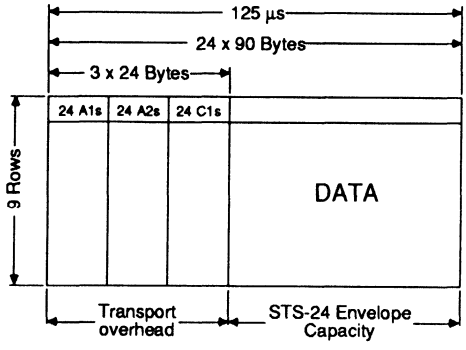
Frame Detector

The SONET frame detector monitors every demultiplexed output byte. If 3 A1 bytes followed by 3 A2 bytes are detected, then a frame confirmation signal is sent off-chip on the ECL output ***FP.*** The rising edge of the ***FP*** pulse occurs 2 byte clock periods after A1 changes to A2 on the demultiplexer parallel data outputs. The ***FP*** pulse width is one byte clock period (refer to demultiplexer waveforms).

The frame detection circuitry also disables the frame recovery circuits once 3 A1 bytes are followed by 3 A2 bytes. The frame detector sends an ***FP*** pulse every frame when 3 A1s are followed by 3 A2s independent of the condition of the input ***OOFN.***



STS-24 Frame



A1s & A2s: SONET Framing Sequence
C1s: STS Frame ID

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{TT}) ..... -3.0 V to +0.5 V
Power Supply Voltage (V_{EE}) ..... V_{TT} +0.7 V to -6.0 V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_c) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

Recommended Operating Conditions

ECL Power Supply Voltage (4), (V_{TT}) ..... -2.1 V to -1.9 V
Power Supply Voltage, (V_{EE}) ..... -5.46 V to -4.94 V
Operating Temperature Range (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

Notes: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{ECLIN}) and V_{ECLIN} must be greater than V_{TT} - 0.5V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.
(4) When using internal ECL 100K reference level.

DC Characteristics

ECL Inputs/Outputs

(Over recommended operating range with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-600	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	V_{IN} = V_{IH} max
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} min

Note: 1) Differential ECL output pins must be terminated identically.

High Speed Inputs and Outputs: CLKI, CLKIN, DO, DON

(Over recommended operating conditions. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for high speed inputs
V_{REF}	Reference level	—	-3.5	—	V	
V_{OH}	Output HIGH voltage	—	-0.9	—	V	Output load, 50 Ω to -2.0 V
V_{OL}	Output LOW voltage	-2.0	-1.8	-1.72	V	Output load, 50 Ω to -2.0 V
ΔV_{OUT}	Output voltage swing	0.6	0.8	1.2	V	Output load, 50 Ω to -2.0 V

Notes: 1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.
2) If a high speed input is used single-ended, a 100pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed outputs must be terminated identically.

High Speed Differential Clock (C0,C0N) Outputs (VS8010.VS8011)

(V_{EE} = -5.2 ± 0.26 V, V_{CC} = GND, T_C = 0° to 70° C, Output load = 50 Ω to -2.0 V.)

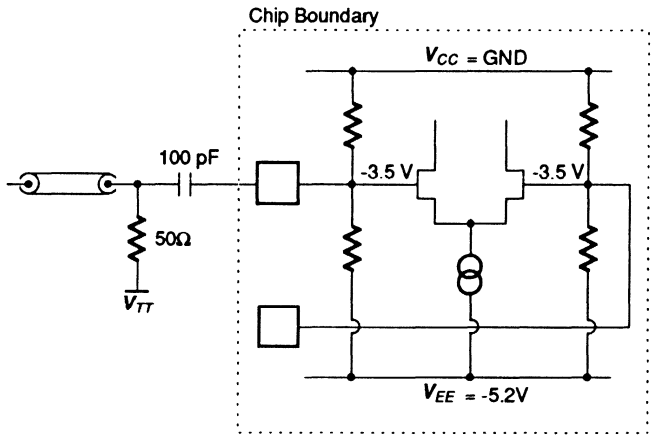
The clock output swing at 1.25 GHz is 400 mVp-p from each output, centered at approximately -1.5 V
The clock output swing at DC is 1.0 Vp-p from each output, centered at approximately -1.5 V

Power Dissipation *(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)*

Parameter	Description	VS8010			VS8011			VS8012			Units
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{EE}	Power supply current from V_{EE}	—	600	720	—	290	350	—	350	420	mA
I_{TT}	Power supply current from V_{TT}	—	700	900	—	300	420	—	400	430	mA
P_D	Power dissipation	—	4.8	5.8	—	2.2	2.8	—	2.8	3.2	W

High Speed Inputs

High speed inputs (clock or data) are intended for single-ended AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs.



VS8010 Example Application:

STS-24 system

The objective of the system is to multiplex and demultiplex 8 data channels at the STS-24 line rate with SONET frame recovery capability. In this example the system is implemented using the two VS8010s as follows:

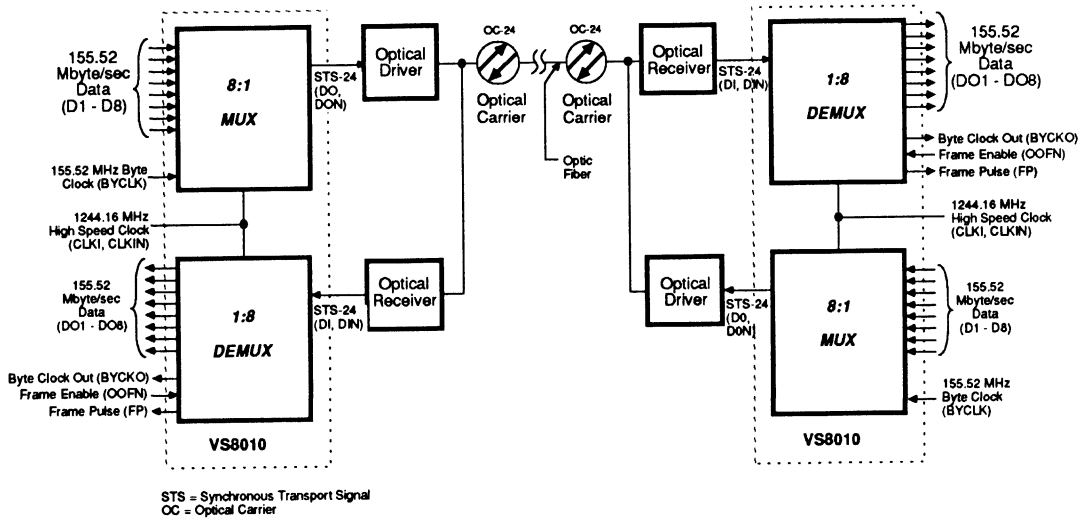
8:1 Multiplexer

Data at a line rate of 155.52 Mbytes/sec is registered at the inputs using the 155.52 MHz byte clock. The 1244.16 MHz clock is used to generate timing signals for the mutiplexing function. The multiplexed output at 1244.16 Mbits/sec is generated at the serial data output (DO, DON) of the VS8010.

1:8 Demultiplexer

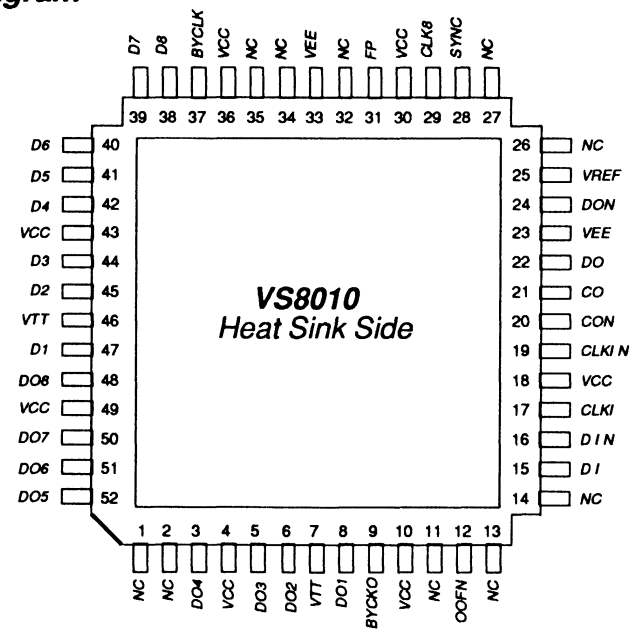
The 1:8 demultiplexer receives serial data at 1244.16 Mbits/sec and generates parallel data at 155.52 Mbytes/sec along with a byte clock output of 155.52 MHz. The demultiplexer also contains the SONET frame recovery and detection circuitry.

During system start-up the ***OOFN*** input receives a falling edge from the system control to recover the SONET frame and align on byte boundaries. Once the frame is aligned, the ***FP*** pulse is generated on every SONET frame. If for any reason the ***FP*** pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the ***OOFN*** input (HIGH to LOW) to recover the SONET frame and align on byte boundaries, thus bringing the system back to a synchronized condition. The ***FP*** pulse begins appearing again on every frame.



SONET STS-24 Section Level Node

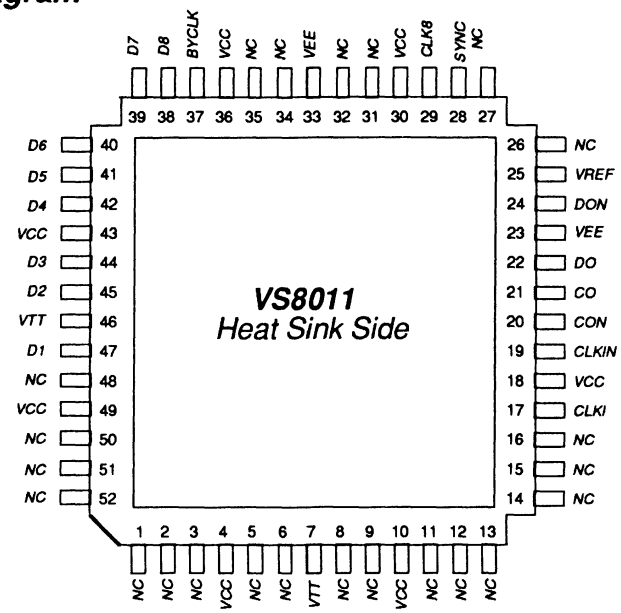
VS8010 Pin Diagram



VS8010 Pin Description

Pin #	Name	I/O	Description
8, 6, 5, 3, 52 - 50, 48	***DO1 - DO8***	O	Parallel ECL data outputs
47, 45, 44, 42 - 38	***D1 - D8***	I	Parallel ECL data inputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
9	***BYCKO***	O	Divide by 8 clock ECL output
37	***BYCLK***	I	Divide by 8 clock ECL input
22, 24	***DO, DON***	O	High speed serial data output
21, 20	***CO, CON***	O	High speed differential clock output
29	***CLK8***	O	Mux divide by 8 clock ECL output
15, 16	***DI, DIN***	O	High speed differential serial data input
12	***OOFN***	I	Frame recovery enable ECL input
31	***FP***	O	Frame detection confirmation ECL output
28	***SYNC***	I	Mux phase alignment enable ECL input
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation
23, 33	V_{EE}		-5.2 V supply for high speed logic
1, 2, 11, 13, 14, 26, 27, 32, 34, 35	***NC***		No connection

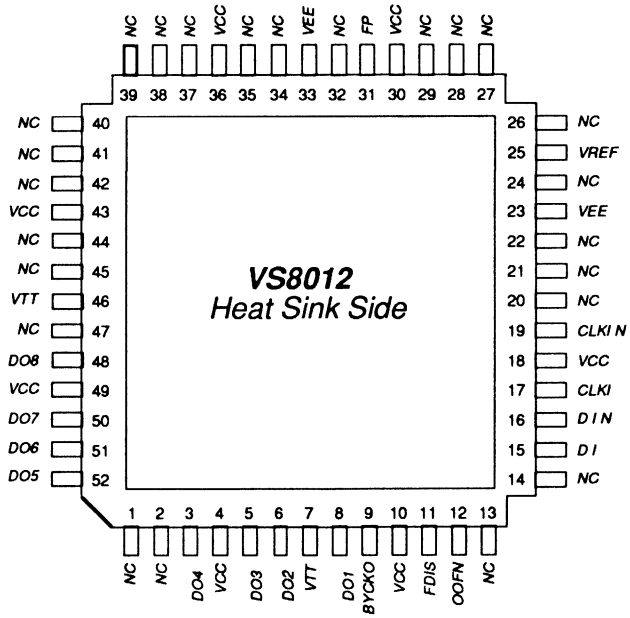
VS8011 Pin Diagram



VS8011 Pin Description

Pin #	Name	I/O	Description
47, 45, 44, 42 - 38	D1 - D8	I	Parallel ECL data inputs
17, 19	CLKI, CLKIN	I	High speed differential clock inputs
37	BYCLK	I	Divide by 8 clock ECL input
22, 24	DO, DON	O	High speed serial data output
21, 20	CO, CON	O	High speed differential clock output
29	CLK8	O	Mux divide by 8 clock ECL output
28	SYNC	I	Mux phase alignment enable ECL input
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation
23, 33	V_{EE}		-5.2 V supply for high speed logic
1 - 3, 5, 6, 8, 9, 11 - 16, 26, 27, 31, 32, 34, 35, 48, 50 - 52	NC		No connection

VS8012 Pin Diagram



VS8012 Pin Description

Pin #	Name	I/O	Description
8, 6, 5, 3, 52 - 50, 48	***DO1 - DO8***	O	Parallel ECL data outputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
9	***BYCKO***	O	Divide by 8 clock ECL output
15, 16	***DI, DIN***	O	High speed differential serial data input
12	***OOFN***	I	Frame recovery enable ECL input
11	***FDIS***	I	Frame recovery disable ECL input
31	***FP***	O	Frame detection confirmation ECL output
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation
23, 33	V_{EE}		-5.2 V supply for high speed logic
1, 2, 13, 14, 20 - 22, 24, 26 - 29, 32, 34, 35, 37 - 42, 44, 45, 47	***NC***		No connection

VS8010DUT Board

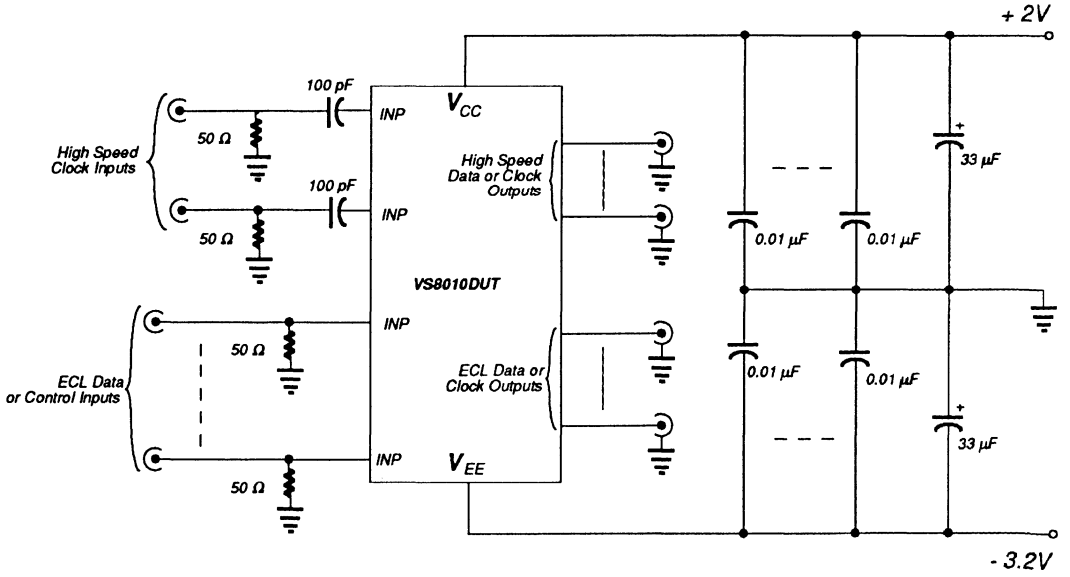
The VS8010DUT is a general purpose circuit board for the VS8010 series which provides a test bed suitable for evaluating the performance characteristics of the VS8010 series in the 52 pin LCC package. The evaluation board is generic to the VS8010 series, and is configured with I/Os which are specific to the VS8010 series.

The figure below is a schematic of this circuit board. This board provides a controlled impedance transmission line for all signals, and suitable decoupling for the power supplies. The signal traces have a characteristic impedance of 50 Ω. All ECL input lines are terminated with 50 Ω (chip resistor) as close to the device package pin as possible. The high speed inputs are also provided with 100 pF blocking capacitors as shown. These capacitors are shorted in applications which require DC connection to these inputs. Signals are launched onto the circuit board and removed by means of SMA coaxial connectors. While the input signals are terminated, the output signals are provided open circuit and are intended to be terminated in the measuring instrument such as an oscilloscope.

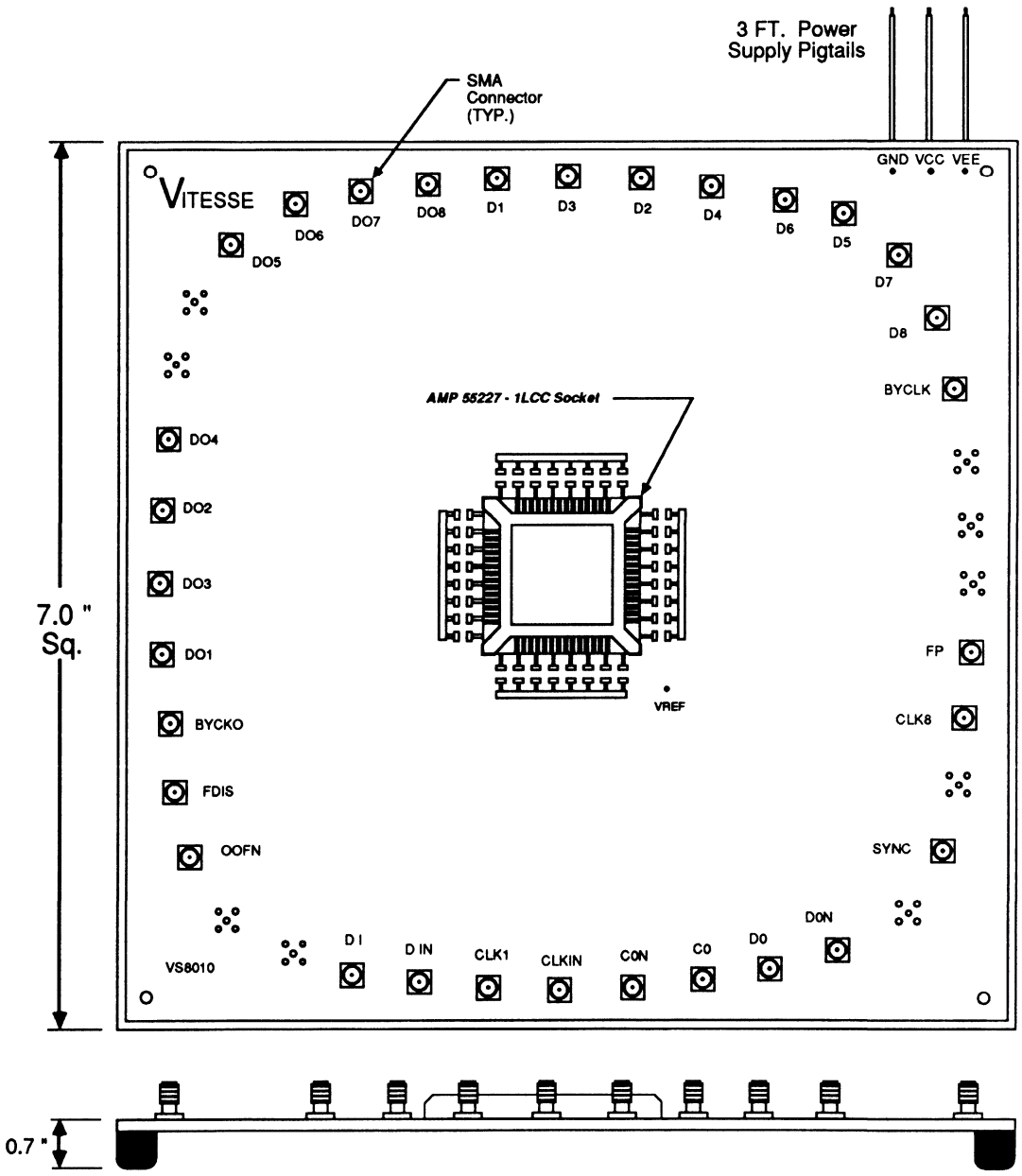
Normally, the VS8010 series operates in an ECL environment with standard ECL power forms: Ø V, -2 V, -5.2 V. In order to simplify interface to standard ground referenced test equipment, however, the circuit board power forms are offset so that the shield connectors are at ground voltage. The figure below shows the arrangement of the power supply decoupling capacitors. There is a 33 µF electrolytic capacitor, as well as several 0.01 µF ceramic capacitors across each power form.

The device socket is an AMP 55227-1 LCC socket and was chosen for minimum inductance and shortest possible stub length. The figure on the next page shows the physical dimensions and the SMA connection labels for the VS8010DUT evaluation board.

VS8010DUT Board Schematic



VS8010DUT Dimensions and Connection Diagram



VS8021/22

2.5 Gb/s SONET 8-Bit Multiplexer/Demultiplexer Chip Set

Features

- Superior performance: serial data up to 2.5 Gb/s
- Compatible with SONET STS-3 to STS-48 applications
- 8-bit wide ECL 100K compatible parallel data I/Os
- Internal self-adjusting clock in the VS8021 for simple clock to parallel data alignment
- SONET frame recovery circuitry incorporated into the VS8022 demultiplexer
- Standard ECL power supplies: V_{EE} = -5.2 V, V_{TT} = -2.0 V
- All data and clock inputs and outputs are differential (inputs can be wired to be driven single-ended)
- 52-pin leaded ceramic chip carrier

Functional Description

The VS8021 and VS8022 are high speed SONET interface devices capable of handling serial data at rates up to 2.5 Gbits/second. These products can be used for STS-3 through STS-48 SONET applications.

These products are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET proces which achieves high speed and low power dissipation. These products are packaged in a ceramic 52-pin leaded ceramic chip carrier. Refer to Section 6, "Packaging" for a complete description of this package. The following are individual descriptions of each product.

VS8021

The VS8021 contains an 8:1 multiplexer and a self-positioning timer. The 8:1 multiplexer accepts 8 parallel differential ECL data inputs ***(D1-D8, D1N-D8N)*** at rates up to 312.5 Mbits/sec and multiplexes them into a serial differential bit stream output ***(DO, DON)*** at rates up to 2.5 Gbits/sec.

The internal timing of the VS8021 is built around the high speed clock (up to 2.5 GHz) delivered onto the chip through a differential input ***(CLKI, CLKIN)***. This signal is subsequently echoed at the high speed differential output ***(CO, CON)***.

The parallel data inputs are clocked to on-chip input registers with an externally supplied differential ECL input ***(BYCLK, BYCLKN)*** operating at the same rate as the data inputs. An internal byte clock, which is a divide by 8 version of the high speed clock, is used to transfer the data to a set of buffer registers. This internal byte clock is brought off chip at the ECL output ***CLK8, CLK8N***.

Internal circuitry monitors the internal and external byte clocks and generates an ***ERR*** signal if a timing violation is detected. This signal can be connected directly to the ***SYNC*** input. An active ***SYNC*** input shifts the VS8021 timing, positioning it properly against the external byte clock, ***CLK8, CLK8N***.

Another divide by 8 version of the high speed clock is brought off chip at ***RCLK, RCLKN***. The phase of this clock is not affected by the self-adjusting circuitry, therefore it can be used as a system reference clock. ***RCLK, RCLKN*** can be used by the system designer to generate ***BYCLK, BYCLKN***. The self-positioning timer and ***RCLK, RCLKN*** allow for the creation of very tight control loops for the VS8021.

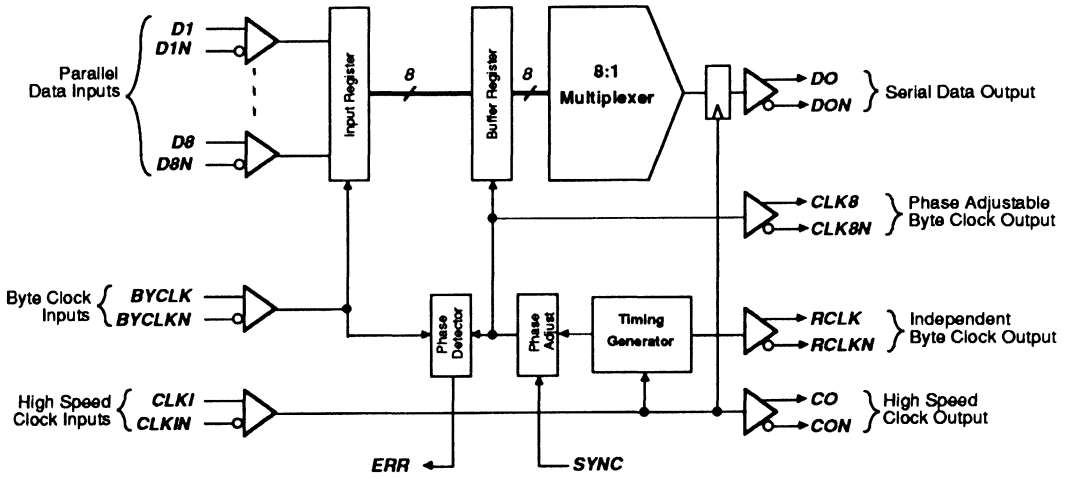
VS8022

The VS8022 contains both a 1:8 demultiplexer and SONET frame recovery circuitry. The 1:8 demultiplex-er accepts a serial data input ***(DI, DIN)*** at rates up to 2.5 Gbits/second and converts it into 8 parallel differential ECL data outputs ***(D1-D8, D1N-D8N)*** at rates up to 312.5 Mbits/sec. Valid parallel data outputs are indicated by the divide by 8 differential

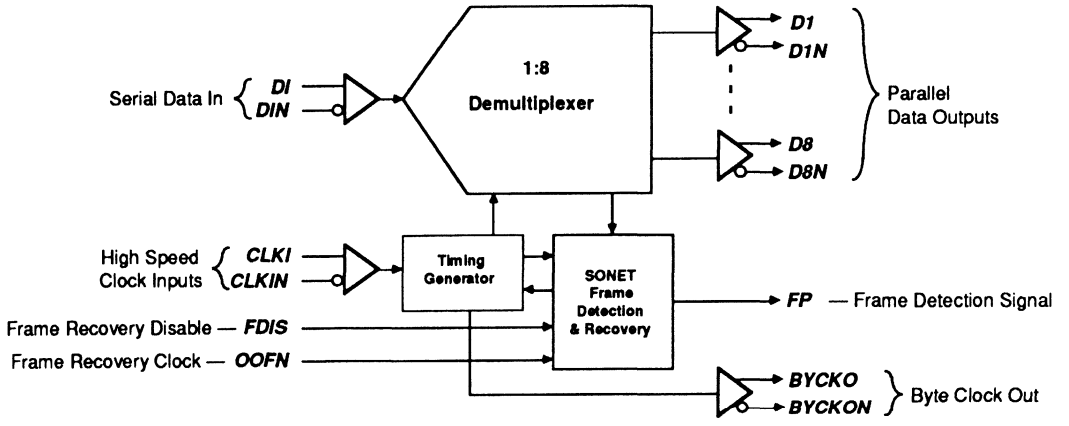
clock outputs ***BYCKO, BYCKON.***

The VS8022 also contains a SONET frame recovery circuit. The frame recovery circuits are enabled by a falling edge on the ***OOFN*** ECL input when the ***FDIS*** input is low. Once enabled the frame recovery circuit starts looking for the SONET framing sequence. Once the frame is detected, the word boundary is realigned, a confirmation signal is sent off-chip through the ***FP*** ECL output and the frame recovery circuits are disabled.

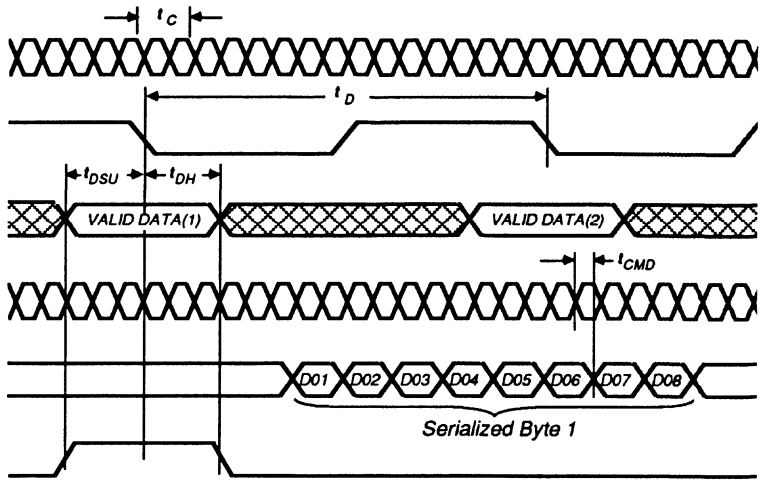
VS8021 Block Diagram



VS8022 Block Diagram



Multiplexer Waveforms (VS8021)



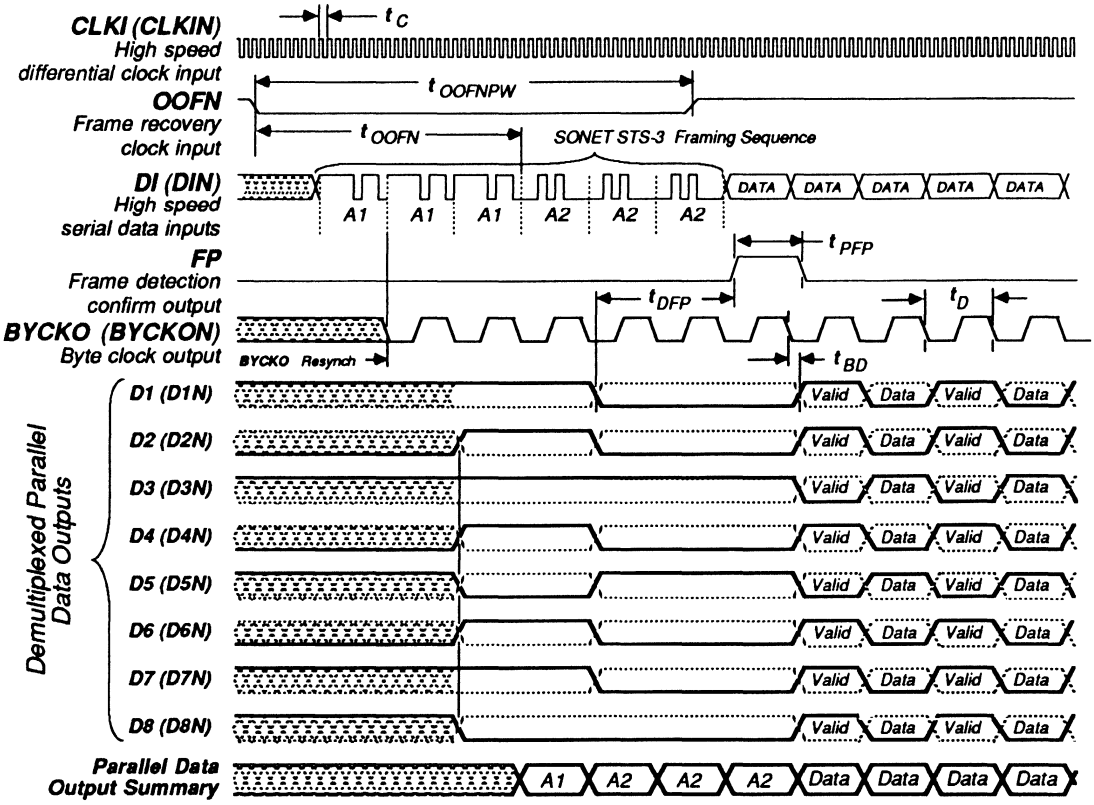
Notes: 1) XXXX = Don't care.
2) ***CLKI (CLKIN)*** period x 8 = ***BYCLK (BYCLKN)*** period

Multiplexer AC Characteristics (VS8021): *Over recommended operating range*

Parameter	Description	MIN	TYP	MAX	Units
t_C	Clock period *	0.4	—	—	ns
t_D	BYTE clock period	3.2	—	—	ns
t_{DSU}	Parallel data set-up time	1.0	—	—	ns
t_{DH}	Data hold time	1.0	—	—	ns
t_{CMD}	High speed clock output (CO, CON) to muxed data output (DO, DON) timing	220	—	350	ps
jitter	CLKI, CLKIN to DO, DON (max-min, (HIGH to LOW), same part, same pin at constant conditions	—	<50	—	ps

* The parts are guaranteed to operate from DC to a maximum frequency of 2.5 GHz.

Demultiplexer Waveforms (VS8022)



NOTE: The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above use an STS-3 framing sequence for convenience, thus valid data is output after the third A2 in the sequence. = Don't ⊘

Demultiplexer AC Characteristics (VS8022): *Over recommended operating range*

Parameter	Description	MIN	TYP	MAX	Units
t_C	Clock period *	0.4	—	—	ns
t_D	BYTE clock period ($t_D = t_C \times 8$)	3.2	—	—	ns
t_{BD}	BYTE clock output to valid data	0.5	1.0	2.0	ns
t_{DFP}	FP rising edge from parallel data output change from A1 to A2 ($t_{DFP} = t_D \times 2$)	—	6.4	—	ns
t_{PFP}	FP pulse width ($t_{PFP} = t_D$)	3.2	—	—	ns
t_{OOFN}	OOFN falling edge before A1 changes to A2 ($t_{OOFN} = t_D \times 4$)	12.8	—	—	ns
t_{OOFNPW}	OOFN pulse width ($t_{OOFNPW} = t_D$)	3.2	—	—	ns
phase margin	Serial data phase timing margin with respect to high speed clock	135	180	—	degrees

* If t_C changes, all the remaining parameters change as indicated by the equations.

VS8022 SONET Frame Recovery and Detection

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000) The first serial bit starts at the left of the byte. The table below shows the number of A1 and A2 bytes in each SONET frame for different line rates. The VS8022 contains a frame recovery circuit and a frame detection circuit.

STS LEVEL	*LINE RATE (Mb/S)*	*# OF A1 BYTES*	*# OF A2 BYTES*
STS-3	*155.520*	*3*	*3*
STS-9	*466.560*	*9*	*9*
STS-12	*622.080*	*12*	*12*
STS-18	*933.120*	*18*	*18*
STS-24	*1244.16*	*24*	*24*
STS-48	*2488.32*	*48*	*48*

Example. STS-48 has 48 A1s and 48 A2s:
$A1_1A1_2A1_3$.....$A1_{48}A2_1A2_2A2_3$.....$A2_{48}$

Frame Recovery Circuit

The frame recovery circuit is designed to scan the serial data stream, looking for the A1 byte. When it finds the A1 pattern, it adjusts internal timing so that the serial data is properly demultiplexed onto the eight parallel outputs. Subsequently, the MSB of the A1 byte will appear in the D1 position and LSB of the A1 byte will appear in the D8 position. This word boundary alignment causes the ***BYCKO, BYCKON*** output to be resynchronized.

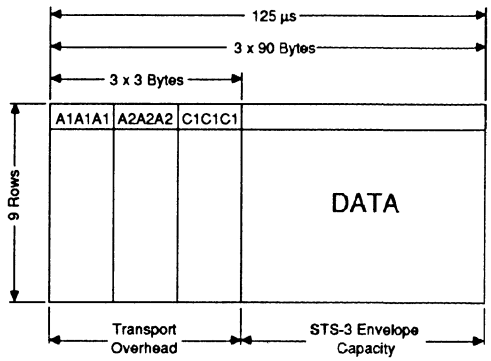
Frame Detection Circuit

The frame detection circuit monitors the demultiplexed data, and senses the boundary between A1 and A2 bytes. This circuit requires a minimum of 2 A2 bytes in order to generate a pulse on the ***FP*** output. This pulse on the ***FP*** output will reset the frame recovery circuit, so that no further resynchronization will occur.

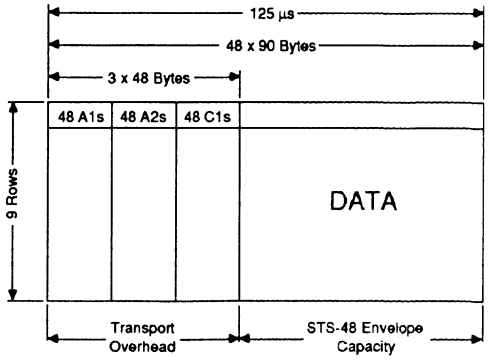
Circuit Operation

The frame recovery circuits are initialized and enabled on the falling edge of the ***OOFN*** ECL input with ***FDIS*** held LOW. The ***OOFN*** pulse must be at least one byte clock period wide. At least 6 byte clock periods must be allowed before the A1/A2 boundary. The circuit requires a minimum of 2 A1 bytes followed by 2 A2 bytes for successful alignment. The first A1 byte is used by the frame recovery circuit to obtain initial word boundary alignment, while the following A1 and 2 A2 bytes are used to generate the ***FP*** pulse, reset the frame recovery circuit, and maintain alignment for the subsequent bit stream. Frame recovery and output alignment will occur only on the first A1 byte following a ***OOFN*** falling edge input. ***FP*** pulses, however, will occur for each A1, A2, A2 sequence detected.

STS-3 FRAME



STS-48 FRAME



A1s & A2s: SONET Framing Sequence
C1s: STS Frame ID

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{TT}) ..... -3.0 V to +0.5 V
Power Supply Voltage (V_{EE}) ..... V_{TT} +0.7 V to -7.0 V
ECL Input Voltage Applied (2), (V_{ECLIN}) ..... -2.5 V to +0.5 V
High Speed Input Voltage Applied (2), (V_{HSIN}) ..... V_{EE} - 0.7 V to V_{CC} + 0.7 V
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_c) ..... -55° to +125°C
Storage Temperature, (T_{STG}) ..... -65° to +150°C

Recommended Operating Conditions

ECL Power Supply Voltage (4), (V_{TT}) ..... -2.1 V to -1.9 V
Power Supply Voltage, (V_{EE}) ..... -5.46 V to -4.94 V
Operating Temperature Range (3), (T) ..... (Commercial) 0° to 70°C, (Industrial) -40° to +85°C

Notes: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) V_{TT} must be applied before any input signal voltage (V_{ECLIN}) and V_{ECLIN} must be greater than V_{TT} - 0.5V.
(3) Lower limit of specification is ambient temperature and upper limit is case temperature.
(4) When using internal ECL 100K reference level.

DC Characteristics

ECL Inputs/Outputs

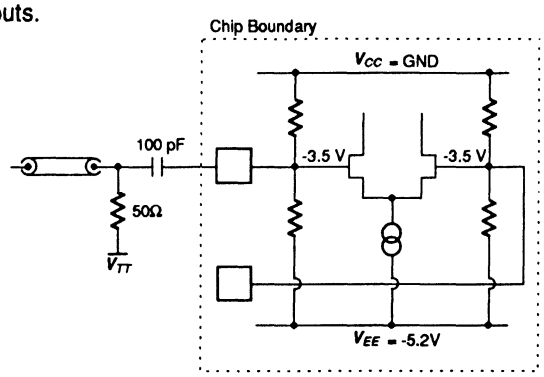
(Over recommended operating range with internal V_{REF}. V_{CC} = GND, output load = 50 Ω to -2.0 V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-925	—	-600	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	-1750	mV	
V_{IH}	Input HIGH voltage	-1040	—	-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}	—	-1600	mV	Guaranteed LOW signal for all inputs
I_{IH}	Input HIGH current	—	10	200	µA	V_{IN} = V_{IH} max
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} min

Note: 1) Differential ECL output pins must be terminated identically.

High Speed Inputs

High speed inputs (clock or data) are intended for single-ended AC coupled operation. Internal biasing will position the reference voltage of approxiamtely -3.5 Volts on both the true and complementary inputs.



DC Characteristics *(continued)*

High Speed Inputs and Outputs:

(Over recommended operating conditions. V_{cc} = GND, Output load = 50Ω to -2.0V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for high speed inputs
V_{REF}	Input reference level	—	-3.5	—	V	
V_{OH}	Output HIGH voltage	—	-0.5	—	V	Output load, 50Ω to -2.0 V
V_{OL}	Output LOW voltage	—	-1.8	—	V	Output load, 50Ω to -2.0 V
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output load, 50Ω to -2.0 V

NOTES: 1) Built in reference generator, the high speed inputs are designed for AC coupling.

2) If a high speed input is used single-ended, a 100pF capacitor must be connected between the unused high speed or complement input and V_{EE}.

3) Differential high speed output pins must be terminated identically.

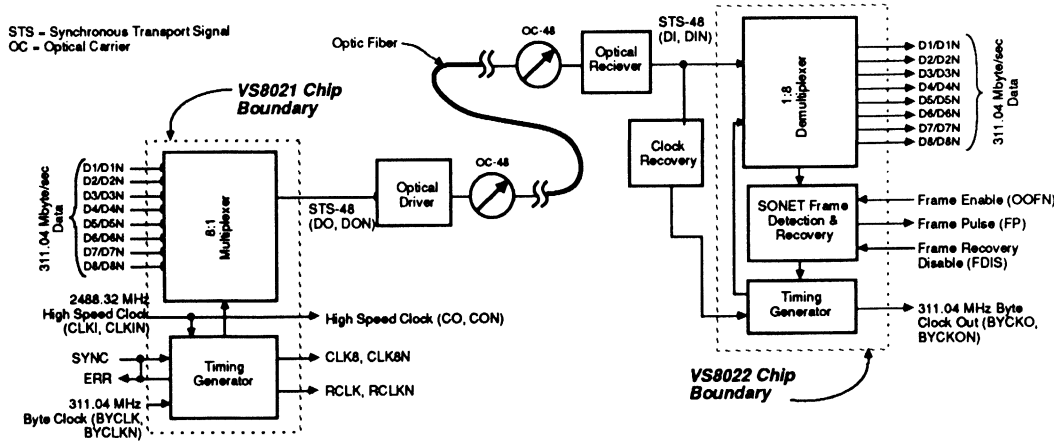
4) ESD protection is not provided for the high speed input pins, therefore, proper procedures should be used when handling this product.

Power Dissipation

(Over recommended operating conditions, V_{cc} = GND, outputs open circuit)

Parameter	Description	VS8021			VS8022			Units
		MIN	TYP	MAX	MIN	TYP	MAX	
I_{EE}	Power supply current from V_{EE}	—	290	360	—	420	480	mA
I_{TT}	Power supply current from V_{TT}	—	400	500	—	400	460	mA
P_D	Power dissipation	—	2.3	2.9	—	3.0	3.6	W

VS8021/VS8022 Example Application: STS-48 SONET System Link



STS-48 SONET System Link

The objective in this example is to multiplex/ demultiplex 8 channels at the STS-48 line rate with SONET frame recovery capability. The system can be implemented using the VS8021 and VS8022 as follows:

8:1 Multiplexer :

Data at a line rate of 311.04 Mbytes/sec is registered at the inputs using the externally provided 311.04 MHz byte clock. ***ERR*** is connected *to* ***SYNC*** for retiming of the input word. The 2488.32 MHz clock is used to generated timing signals for the mutiplexing function. The muxed output at 2488.32 Mbits/ sec is generate at the serial data output of VS8021.

1:8 Demultiplexer:

The 1:8 demultiplexer receives serial data at 2488.32 Mbits/sec and generates parallel data at 311.04 Mbytes/sec along with a byte clock output of 311.04 MHz. The demux also has the SONET frame recovery and detection circuitry.

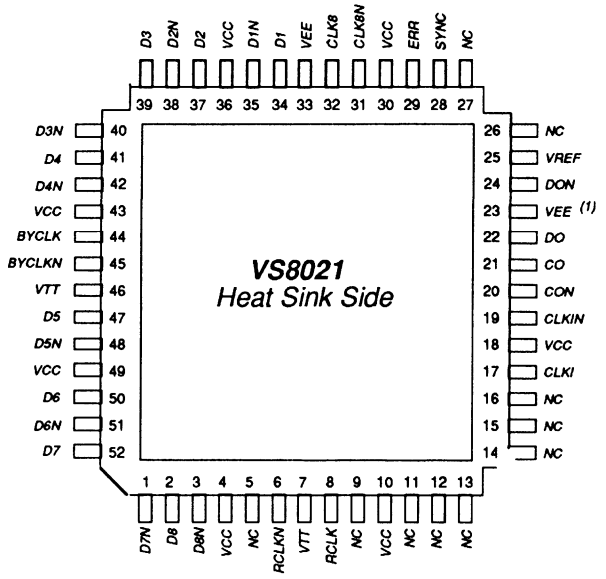
During system start-up ***OOFN*** input receives a falling edge from the system control to recover the SONET frame and align on byte boundaries. Once the frame is aligned, the ***FP*** pulse is generated on every SONET frame. If for any reason the ***FP*** pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the ***OOFN*** input (High to Low) to recover the SONET frame and align on byte boundaries, bringing the system back to a synchronized condition. After synchronization is achieved, the ***FP*** pulse starts again on every frame.

ESD Protection

Electrostatic discharge protection is provided for ECL I/O's and high speed clock and data I/O's to the following minimum limits:

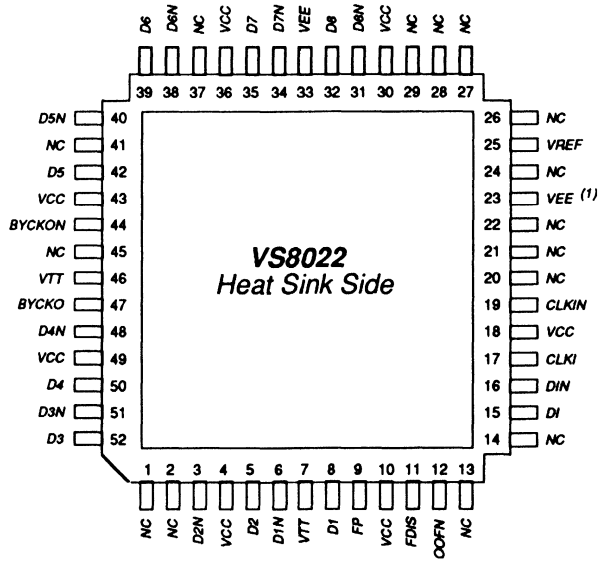
ECL I/O's, High Speed Clock and Data O's . ***1000V***
High Speed Clock and Data I's ***500V***

VS8021 Pin Configuration



Pin #	Name	I/O	Description
1-3,34,35,37-42,47,48,50-52	***D1-D8, D1N-D18***	I	Parallel ECL differential data inputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
44, 45	***BYCLK, BYCLKN***	I	Divide by 8 clock ECL input
22, 24	***DO, DON***	O	High speed serial data output
21, 20	***CO, CON***	O	High speed differential clock output
31, 32	***CLK8, CLK8N***	O	Phase adjustable ÷8 differential ECL clock output
6, 8	***RCLK, RCLKN***	O	Independent ÷8 differential ECL clock output
29	***ERR***	O	Error detection ECL output
28	***SYNC***	I	Error correction ECL input
25	V_{REF}		ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation
23[(1)], 33	V_{EE}		-5.2 V supply for high speed logic
5, 9, 11 - 16, 26, 27	***NC***		No connection

VS8022 Pin Configuration



Note: 1) Pin #23 on both parts is connected to the heat sink.
Connect to VEE or most negative chip voltage.

Pin #	Name	I/O	Description
3,5,6,8,31,32, 34,35,38-40,42, 48, 50-52	***D1-D8, D1N-D8N***	O	Parallel ECL differential data outputs
17, 19	***CLKI, CLKIN***	I	High speed differential clock inputs
44, 47	***BYCKO, BYCKON***	O	Divide by 8 clock ECL outputs
15, 16	***DI, DIN***	I	High speed differential serial data inputs
12	***OOFN***	I	Frame recovery clock enable ECL input
25	V_{REF}	I	ECL reference level input
4, 10, 18, 30, 36, 43, 49	V_{CC}		Ground connection
7, 46	V_{TT}		-2.0 V supply for internal reference generation
23[1], 33	V_{EE}		-5.2 V supply for high speed logic
1,2,9, 11, 13,14,20-22,24,26-29, 37,41,45	***NC***		No connection

VSC864

Gallium Arsenide 64 x 64 Crosspoint Switch

Features:

- Superior performance .....200 Mb/s
- Duty-cycle distortion @ 200Mb/s. 10%
- Operating range. .....-40° to +85° C
- Power dissipation. .....8 Watts (Typical)
- Clocked or flow-through operation
- ECL F100K compatible inputs and outputs
- Output to output skew: < 1500 ps
- Output drive capability 25Ω
- Single power supply. .....-2 V ± 5%
- Package. .....344-pin ceramic LDCC
- Full diagnostic monitors
- Cascadable to larger systems

Introduction

The VSC864 is a 64 x 64 crosspoint switch intended for high speed (up to 200 Mb/s) digital data communications applications. This product has 64 data inputs and 64 data outputs. Any input can be multiplexed to any, some, or all outputs. High speed digital data up to 200 Mb/s can be switched with less than 10% pulse width distortion. In broadcast mode, any two outputs will exhibit less than 1500 ps of skew. All interfaces are fully compatible with ECL F100K logic levels. The VSC864 requires only a single -2 V power supply.

A separate Q bus is provided to allow observation of individual internal multiplexer address latches. Since the VSC864 outputs are capable of driving 25Ω double-terminated busses with cutoff drivers, the device can be cascaded to form larger crosspoint switches. The VSC864 Crosspoint Switch can be operated in either flow-through or synchronous mode by use of internal input and output data registers. In flow-through mode the data propagation delay is less than 7.5 ns.

The individual address registers in the VSC864 are double buffered. A local strobe signal is used to load an individual address for each output pin. A global strobe is used to simultaneously activate all 64 destination addresses.

This product is ideal for high speed digital applications including data distribution for telecommunications, computer network and mutiprocessor switching, and test equipment. In a telecommunications SONET application, for example, the VSC864 can be used as an STS-3 protection switch, or in the fabric of a large switching system.

The VSC864 is packaged in a 344 pin ceramic LDCC package and typically dissipates less than 8 W. Refer to Section 6, "Packaging" for a complete description of this package. This product is fabricated using the Vitesse H-GaAs™, E/D MESFET process which achieves high speed and low power dissipation.

Functional Description

The VSC864 may be used to connect any one of 64 inputs to any combination of 64 output channels, according to a user defined bit pattern stored in each channel's control latch.

During normal operation, signals flow from inputs (I_0 - I_{63}) to output channels (Z_0 - Z_{63}) through sixty-four, 64:1 multiplexers. The traffic pattern is controllable by data previously stored in sixty-four 7-bit control registers with each register corresponding to an output channel. The first 6 least significant bits in each control register are reserved for designating the MUX input which will be connected to its corresponding output, the most significant bit is used to tri-state this output if desired. The 6 LSBs are a binary numerical representation of the input channel selected (i.e., 000000 corresponds to I_0, 000001 corresponds to I_1, etc.).

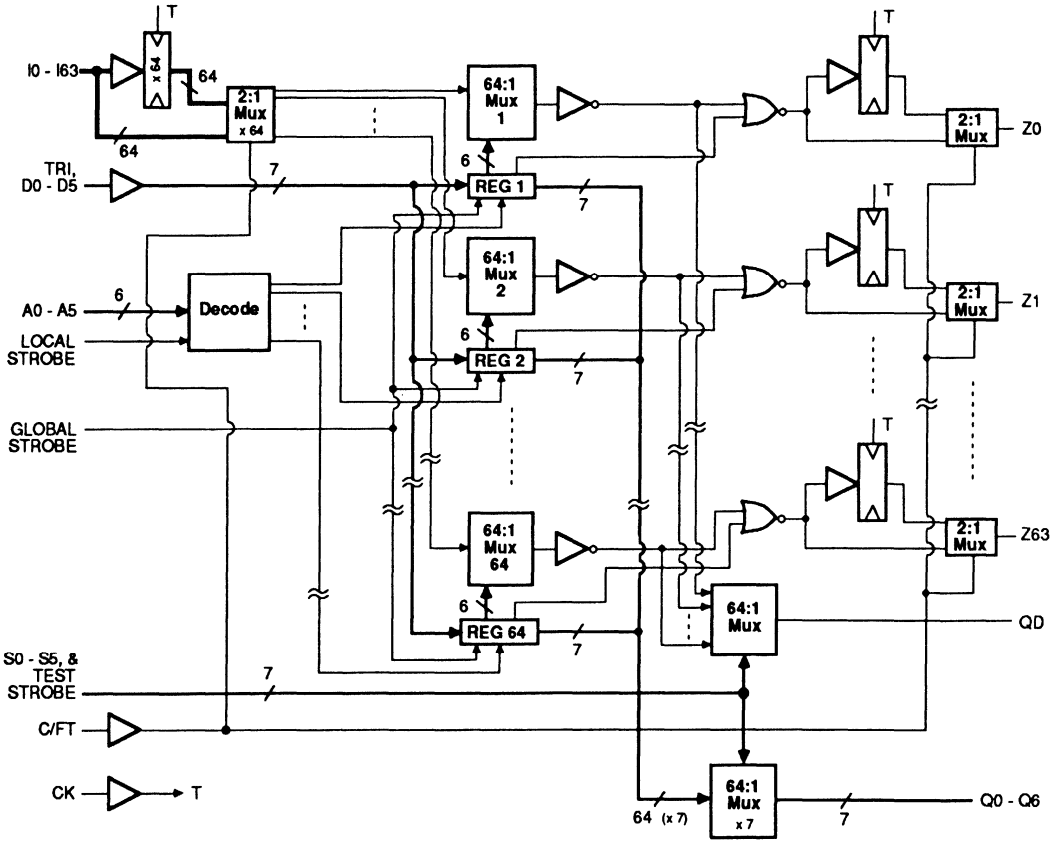
The Write mode is used to alter any one or all signal paths. During Write mode, inputs A_0 - A_5

select which output channel's control register will be altered (also by a binary numerical representation). Inputs D_0- D_5 describe the new input signal to be selected for that channel. When a high pulse is applied to ***LOCAL STROBE***, D_0- D_5 and the ***TRI*** bit is transferred into a holding latch. After some or all control registers are programmed, a high pulse is applied to ***GLOBAL STROBE*** to transfer the information from the holding latch into all the control registers. In this way the entire crosspoint switch can be reconfigured simultaneously.

The Read mode is a diagnostic feature used to examine the data stored in any one control register and its corresponding 64:1 multiplexer output. The control register to be examined is selected by inputs S_0- S_5 (by a binary numerical representation). When a high pulse is applied to the ***TEST STROBE***, the contents of the selected control register will be displayed at the Q_0- Q_6 outputs and the corresponding 64:1 mux output will appear at the ***QD*** output. When ***TEST STROBE*** is "low" the Q bus is tri-stated (low).

The VSC864 can be configured to run in either synchronous clocked mode or asynchronous flow-through mode. This feature is controlled by the ***C/FT*** input. When ***C/FT*** is high, the chip is in clocked mode and will require an input clock at its ***CK*** pin. In this mode all input and output data is registered. When ***C/FT*** is low the chip is in flow-through mode and will ignore the ***CK*** input. In all modes, the outputs on the monitor bus (Q_0- Q_6, and ***QD***), and all inputs other than input data (I_0 - I_{63}) are not registered by the master clock ***(CK)***.

Functional Diagram



Absolute Maximum Ratings (1)

Power Supply Voltage (ECL), V_{TT} potential to GND ..... -2.5V to +0.5V
Input Voltage Applied, $V_{IN\ ECL}$ ..... +0.5V to V_{TT}
Output Current, I_{OUT},(DC, output HI) ..... 50 mA
Z_0-Z_{63}, ECL Data Output Current, I_{DOUT},(DC, output HI) ..... 25 mA
Maximum Junction Temperature, T_j ..... 150°C
Case Temperature Under Bias, T_c ..... -55° to +125°C
Storage Temperature (ambient), T_{STG} ..... -65°C to +150°C

Recommended Operating Conditions

ECL Supply Voltage, V_{TT} ..... -2.0V ± 5%
Commecial Operating Temperature Range, T^2 ..... 0° to 70°C
Industrial Operating Temperature Range, T^2 ..... -40° to 85°C

Note:

(1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC Characteristics

ECL Inputs/Outputs:

(Over recommended commercial operating conditions. V_{CC} = V_{CCA} = GND, Output load 25Ω to V_{TT})

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	V_{IN} = V_{IH} (max)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	or V_{IL} (min), V_{TT} = -2.0V
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	V_{IN} = V_{IH} max
I_{IL}	Input LOW current	-50	—	—	µA	V_{IN} = V_{IL} min
I_{TT}	Supply current	—	4	6	A	V_{TT} = -2.10V

AC Timing Characteristics:

(Over recommended commercial operating conditions. V_{CC} = V_{CCA} = GND. Output load 25Ω to V_{TT}.)

Flow-Through Mode

Parameters	Description	Min	Typ	Max	Units	Conditions
f_{MAX}	Maximum data rate	—	—	200	Mb/s	—
t_{DR}	Propagation delay (rising)	5500	—	7500	ps	—
t_{DF}	Propagation delay (falling)	5000	—	7500	ps	—
—	Duty cycle distortion	—	10	—	%	at 200 Mb/s
skew	Output to output skew	1500	—	2400	ps	on a given part

AC Timing Characteristics (continued):

(Over recommended commercial operating conditions. $V_{CC} = V_{CCA} = GND$.

Clocked Mode

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{ISU}	Input data set-up time	-1900	—	-2500	ps	—
t_{IH}	Input data hold time	3100	—	3600	ps	—
t_{CZR}	Clock to output delay (rising)	5900	—	7000	ps	—
t_{CZF}	Clock to output delay (falling)	5000	—	6700	ps	—
skew	Output to output skew	1000	—	1500	ps	On a given part

Write Mode

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Condition*
t_{RECON}	Reconfiguration time	—	—	650	ns	64 channel reconfig
t_{ALSSU}	A bus to ***LOCAL STROBE*** set-up time	-300	—	-100	ps	—
t_{ALSH}	A bus to ***LOCAL STROBE*** hold time	-1600	—	-700	ps	—
t_{DLSSU}	D bus to ***LOCAL STROBE*** set-up time	-900	—	400	ps	—
t_{DLSH}	D bus to ***LOCAL STROBE*** hold time	1	—	2	ns	—
t_{GLSU}	***GLOBAL STROBE*** to ***LOCAL STROBE*** set-up time	5	—	—	ns	—
t_{GS}, t_{LS}, t_{TS}	***GLOBAL STROBE***, ***LOCAL STROBE***, and ***TEST STROBE*** pulse widths	5	—	—	ns	—
t_{GLH}	***GLOBAL STROBE*** to ***LOCAL STROBE*** hold time	5	—	—	ns	—
t_{GSZ}	***GLOBAL STROBE*** to valid output (flow-thrrough mode)	5	—	10	ns	—
t_{CGSU}	***CLK*** to ***GLOBAL STROBE*** set-up time (clocked mode)	5	—	—	ns	—
t_{GCL}	***GLOBAL STROBE*** to ***CLK*** hold time (clocked mode)	5	—	—	ns	—

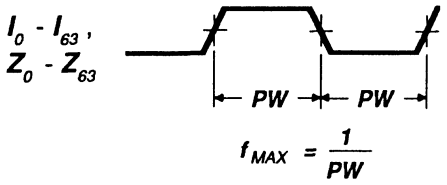
Read Mode

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{TSSU}	S bus to ***TEST STROBE*** set-up time	5	—	—	ns	—
t_{TSSH}	S bus to ***TEST STROBE*** hold time	5	—	—	ns	—
t_{DTSQ}	***TEST STROBE*** to Q bus delay	—	—	10	ns	—

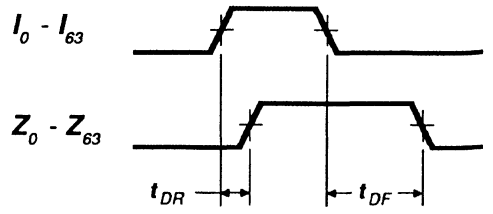
AC Timing Waveforms

Flow-Through Mode

1. Maximum Data Rate, f_{MAX}

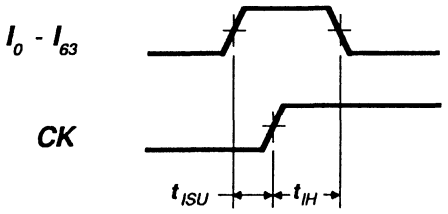


2. Propagation Delay

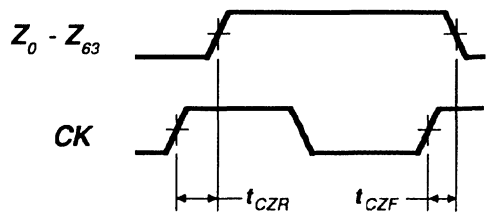


Clocked Mode

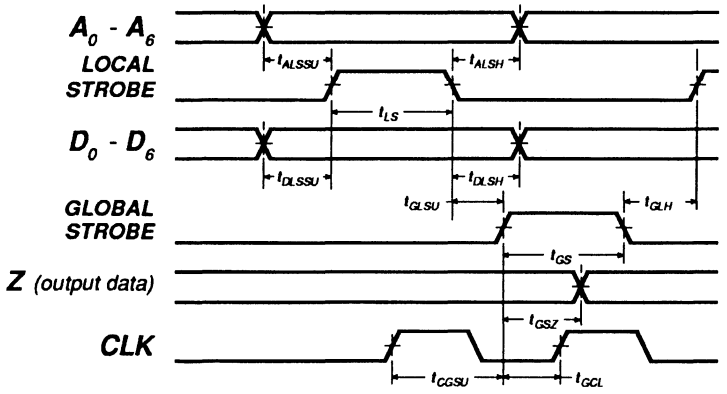
1. Input Data Set-up & Hold Times



2. Clock to Output Delay



Write Mode

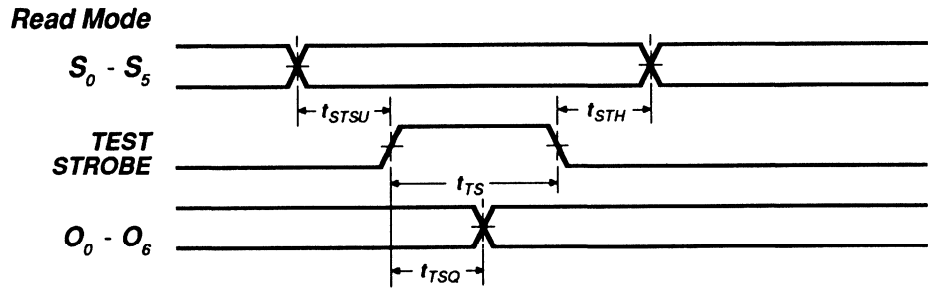


A address setup and hold relative to ***LOCAL STROBE***.

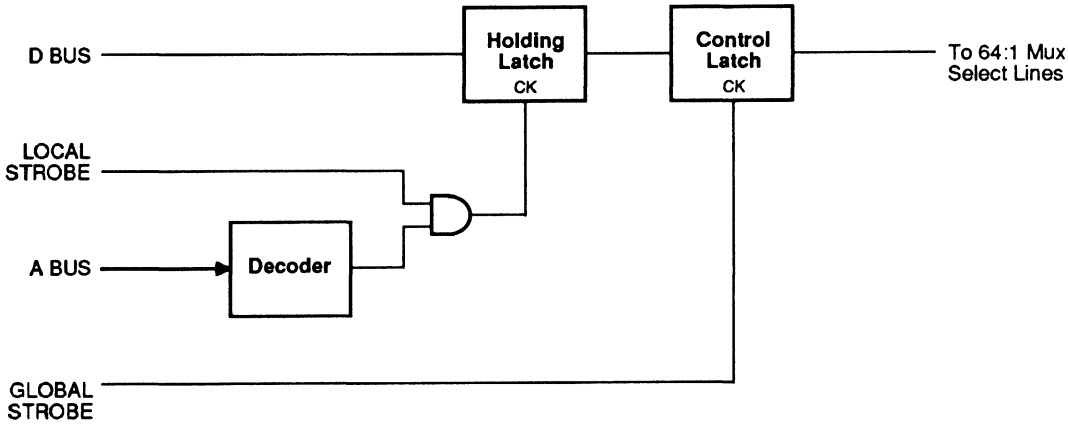
D data setup and hold relative to ***LOCAL STROBE***.

LOCAL STROBE to ***GLOBAL STROBE*** timing relationship.

CLOCKED MODE - ***GLOBAL STROBE*** to ***CLK*** timing relationship.



Block Diagram of Internal Write Mode Circuits



Pin Description

Pin #	Name	I/O	Description
12-16, 20-30, 35-45, 49-53, 184-188, 192- 202, 207-217, 221-225	I_0 - I_{63}	I	The 64 ECL signal inputs.
11	***TRI***	I	ECL input containing Tristate data to be loaded into a 64:1 Mux holding latch. (Tristate = HIGH) Combined with a control register's destination address. Used to tristate the corresponding output.
5-10	D_0 - D_5	I	ECL inputs containing the destination address to be loaded into the 64:1 Mux holding latch.
178-183	A_0 - A_5	I	ECL inputs containing the address of the 64:1 Mux holding/control latch to be programmed.
177	***LOCAL STROBE***	I	Active HIGH, ECL input used to load the D0-D5 and TRI data into the 64:1 Mux holding latch.
34	***GLOBAL STROBE***	I	Active HIGH, ECL input used to load destination addresses to all 64:1***S*** Mux control latches simultaneously from the data contained in their corresponding holding latches.
54-59	S_0 - S_5	I	ECL inputs containing the address of the control latch to be observed at the QD output when the TEST STROBE is HIGH.
60	***TEST STROBE***	I	Active HIGH, ECL input used to enable Test Mode and observation of a selected 64:1 Mux control latch's destination address.
206	***C/FT***	I	ECL input used to enable Clocked or Flow-through Mode (Clocked = HIGH / Flow-Thru = LOW).
203	***CK***	I	ECL clock input for Clocked Mode.
68, 71, 73, 78, 80, 83, 85, 88, 92, 95, 97, 100, 102, 107, 109, 112, 126, 129, 131, 136, 138, 141,143, 148, 150, 153, 155,158, 162, 165, 167, 170, 240, 243, 245, 250, 252, 255, 257, 260, 264, 267, 269, 272, 274, 279, 281, 284, 298, 301, 303, 308, 310, 313, 315, 320, 322, 325, 327, 330, 334, 337, 339, 342	Z_0 - Z_{63}	O	The 64 ECL signal outputs.
296	***QD***	O	ECL output used to observe the contents of a selected 64:1 Mux control latch's destination address in Test Mode.
114, 117, 121, 124, 286, 289, 293	Q_0 - Q_6	O	ECL outputs containing the selected 64:1 Mux control register's destination address in Test Mode.
3, 17, 32, 47, 61, 76, 90, 104, 118, 132, 146, 160, 175, 189, 204, 219, 233, 248, 262, 276, 290, 304, 318, 332	V_{CC}		ØV ground connection for internal logic.
2, 63, 69, 74, 81, 86, 93, 98, 103, 110, 115, 122, 127, 134, 139, 144, 151, 156, 163, 168, 174, 235, 241, 246, 253, 258, 265, 270, 275, 282, 287, 294, 299, 306, 311, 316, 323, 328, 335, 340	V_{CCA}		ØV 'dirty' ground connection for outputs.
4, 18, 33, 48, 62, 77, 91, 105, 119, 133, 147, 161, 176, 190, 205, 220, 234, 249, 263, 277, 305, 319, 333	V_{TT}		-2V supply connection.
291	V_{SUB}		-2V supply connection to substrate (most negative supply).
1, 19, 31, 46, 64-67, 70, 72,			No connection

Pin Description (cont.)

Pin #	Name	I/O	Description
75, 79, 82, 84, 87, 89, 94, 96, 99, 101, 106, 108, 111, 113, 116, 120, 123, 125, 128, 130, 135, 137, 140, 142, 145, 149, 152, 154, 157, 159, 164, 166, 169, 171-173, 191, 218, 226-232, 236-239, 242, 244, 247, 251, 254, 256, 259, 261, 266, 268, 271, 273, 278, 280, 283, 285, 288, 292, 295, 297, 300, 302, 307, 309, 312, 314, 317, 321, 324, 326, 329, 331, 336, 338, 341, 343, 344			

Pin Identification

Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin#	Name	Pin #
I_0	12	I_{22}	26	I_{44}	41	D_2	7	Z_6	85	Z_{28}	162	Z_{50}	303
I_1	225	I_{23}	211	I_{45}	196	D_3	8	Z_7	88	Z_{29}	165	Z_{51}	308
I_2	13	I_{24}	27	I_{46}	42	D_4	9	Z_8	92	Z_{30}	167	Z_{52}	310
I_3	224	I_{25}	210	I_{47}	195	D_5	10	Z_9	95	Z_{31}	170	Z_{53}	313
I_4	14	I_{26}	28	I_{48}	43	A_0	183	Z_{10}	97	Z_{32}	240	Z_{54}	315
I_5	223	I_{27}	209	I_{49}	194	A_1	182	Z_{11}	100	Z_{33}	243	Z_{55}	320
I_6	15	I_{28}	29	I_{50}	44	A_2	181	Z_{12}	102	Z_{34}	245	Z_{56}	322
I_7	222	I_{29}	208	I_{51}	193	A_3	180	Z_{13}	107	Z_{35}	250	Z_{57}	325
I_8	16	I_{30}	30	I_{52}	45	A_4	179	Z_{14}	109	Z_{36}	252	Z_{58}	327
I_9	221	I_{31}	207	I_{53}	192	A_5	178	Z_{15}	112	Z_{37}	255	Z_{59}	330
I_{10}	20	I_{32}	35	I_{54}	49	S_0	54	Z_{16}	126	Z_{38}	257	Z_{60}	334
I_{11}	217	I_{33}	202	I_{55}	188	S_1	55	Z_{17}	129	Z_{39}	260	Z_{61}	337
I_{12}	21	I_{34}	36	I_{56}	50	S_2	56	Z_{18}	131	Z_{40}	264	Z_{62}	339
I_{13}	216	I_{35}	201	I_{57}	187	S_3	57	Z_{19}	136	Z_{41}	267	Z_{63}	342
I_{14}	22	I_{36}	37	I_{58}	51	S_4	58	Z_{20}	138	Z_{42}	269	Q_0	114
I_{15}	215	I_{37}	200	I_{59}	186	S_5	59	Z_{21}	141	Z_{43}	272	Q_1	117
I_{16}	23	I_{38}	38	I_{60}	52	Z_0	68	Z_{22}	143	Z_{44}	274	Q_2	121
I_{17}	214	I_{39}	199	I_{61}	185	Z_1	71	Z_{23}	148	Z_{45}	279	Q_3	124
I_{18}	24	I_{40}	39	I_{62}	53	Z_2	73	Z_{24}	150	Z_{46}	281	Q_4	286
I_{19}	213	I_{41}	198	I_{63}	184	Z_3	78	Z_{25}	153	Z_{47}	284	Q_5	289
I_{20}	25	I_{42}	40	D_0	5	Z_4	80	Z_{26}	155	Z_{48}	298	Q_6	293
I_{21}	212	I_{43}	97	D_1	6	Z_5	83	Z_{27}	158	Z_{49}	301		

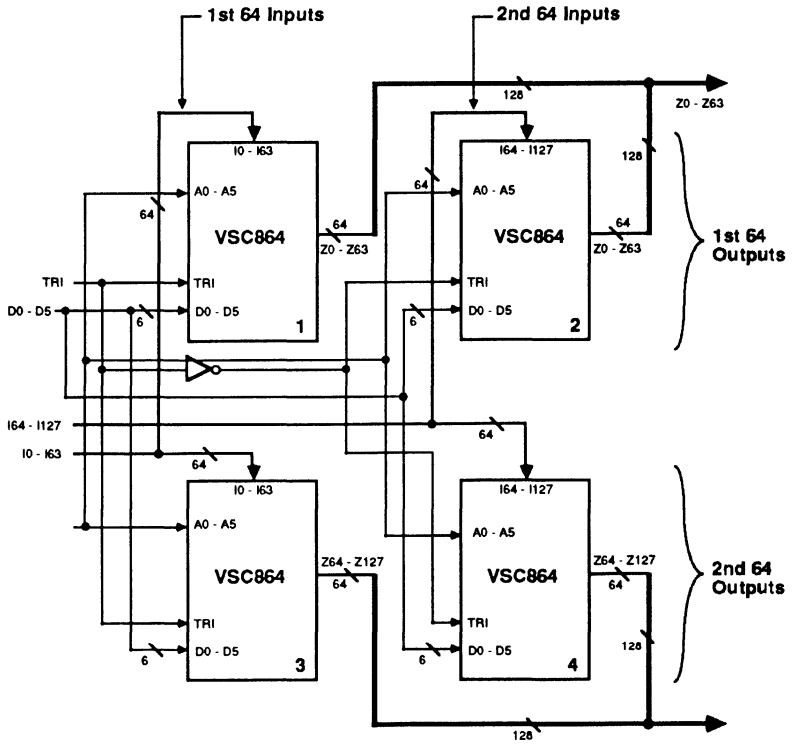
Expandability

The VSC864 can be expanded to larger crosspoint switches by configuring it so that any input can be multiplexed to any output. The figure below is an example of a 128 x 128 crosspoint switch. The top two VSC864s (1&2) correspond to the first 64 outputs and the bottom two VSC864s (3&4) correspond to the last 64 outputs. The VSC864s on the left (1&3) correspond to the first 64 inputs, and the two VSC864s on the right (2&4) correspond to the last inputs. All like outputs are then joined to form a 128 bit Z output bus. The ability of the VSC864 to tri-state its outputs will prevent contention on the Z bus.

The ***TRI*** input is configured such that when it is active on the left hand chips (which are responsible for routing the first 64 inputs) it is inactive on the two right hand chips (which are re–sponsible for routing the last 64 inputs). The TRI input thus functions as the MSB of a 7-bit channel address word (A-bus plus TRI). Chips can share A-bus information. The destination (D) bus can be shared among the four chips with the local strobe for each device being used to select which output address gets reconfigured.

The layout and placement of the VSC864 is such that inputs are on the top and bottom of the chip and outputs are to the right and left. In this way a PC board design for a large crosspoint is facilitated.

In the read mode tri-stateability on the Q-bus can be controlled with the ***TEST STROBE*** input. A "low" level on this input will tri-state its corresponding Q-bus. In this way the Q-bus from all chips can be wire-OR'ed. Individual ***TEST STROBE*** signals to each chip, however, are required.



VS12G422T

256 x 4 Static RAM

Features

- 256 words by 4-bit static RAM for cache and control store applications
- Very fast: Choice of 4, 5, and 6 ns maximum address access times
- TTL compatible inputs and outputs
- Single +5.0 Volt power supply
- Very low sensitivity to radiation
- Standard 22-pin DIP
- Fully static operation - equal access and cycle times
- Pin compatible with standard silicon -422 and -122 products

Functional Description

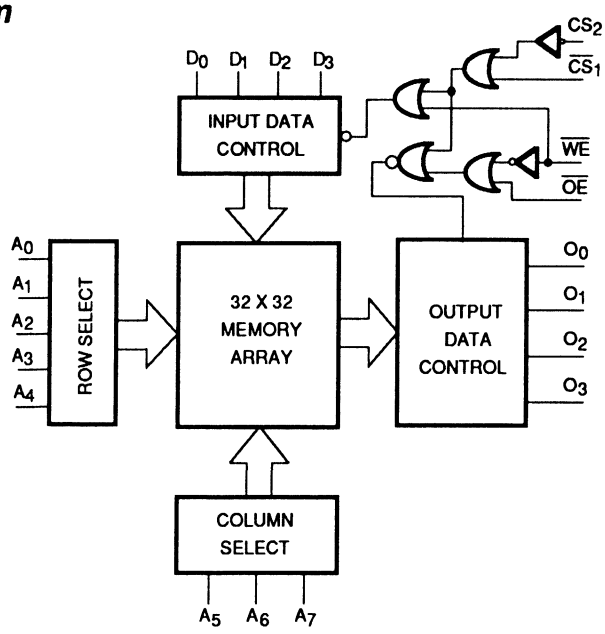
The Vitesse VS12G422T is a very high speed, fully decoded 1024-bit read write static random access memory organized as 256 words by 4 bits. All inputs and outputs of this RAM is TTL compatible and operation is from a standard +5.0 Volt power supply.

Fully static asynchronous internal circuits are used, which require no clocks or refreshing for operation. Memory expansion is provided by an active LOW chip select input ($\overline{CS_1}$), an active HIGH chip select input (CS_2) and three-state outputs. Due to its static operation, the VS12G422T offers equal read and write cycle times, which further simplifies system design.

This RAM is packaged in a standard 22-pin DIP. Refer to Section 6, "Packaging" for a complete description of this package.

The high speed and standard pinout of the VS12G422Tmakes it ideal for both existing and new designs in cache memory, signal processing, and video applications where access time is the critical parameter. The low sensitvity to radiation of this product makes it highly suitable for aerospace applications where high radiation tolerance is necessary. The VS12G422T is fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation.

Block Diagram



Truth Table

Inputs				Output	Mode
$\overline{OE}$	$\overline{CS_1}$	CS_2	$\overline{WE}$		
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V) *X = Don't Care (HIGH or LOW)*
L = LOW Voltage Level (0.4 V) *HIGH Z = High-Impedence*

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{CC}) ..... -0.5 V to +6.0 V
Input Voltage Applied, (V_{IN}) ..... -1.0 V to +7.0 V
Input Current, (I_{IN}), (DC, output LOW) ..... -30 to +30 mA
Output Current, (I_{OUT}), (DC, output LOW) ..... 20 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature(2), (T_{STG}) ..... -65° to +150°C

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) ..... 4.75 to 5.25 V
Operating Temperature Range (2). ..... 0° to +70°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.
(2) Both lower and upper limits of specification are case temperatures.

DC Characteristics *(Over recommended operating conditions)*

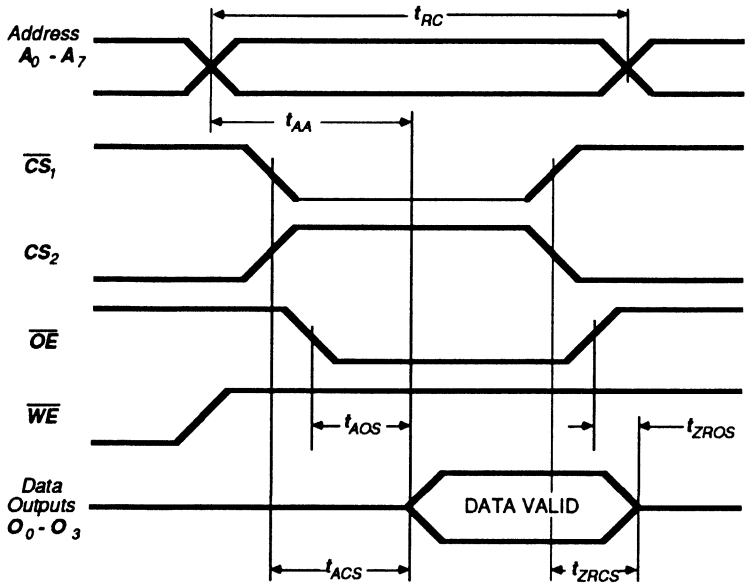
		Commercial Range				
		5,6 ns		4 ns		
Parameters	Description	Min	Max	Min	Max	Test Conditions
V_{OH}	Output HIGH voltage	2.4 V	—	2.4 V	—	V_{CC} = MIN, I_{OH} = -5.2 mA
V_{OL}	Output LOW voltage	—	0.5 V	—	0.5 V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{IH}	Input HIGH voltage	2.0 V	—	2.0 V	—	
V_{IL}	Input LOW voltage	—	0.8 V	—	0.8 V	
I_{IX}	Input LOAD current	-100 µA	100 µA	-100 µA	100 µA	$GND \le V_{IN} \le V_{CC}$
V_{CD}	Input diode clamp voltage (1)	-1.0 V	V_{CC}+1	-1.0 V	V_{CC}+1	I_{IN} = ± 30 mA
I_{OZ}	Output current (HIGH-Z)	-1.0 mA	1.0 mA	-1.0 mA	1.0 mA	$V_{OL} \le V_{OUT} \le V_{OH}$ Output Disabled
I_{CC}	Power supply current (from V_{CC})	—	250 mA	—	350 mA	V_{CC} = MAX, I_{OUT} = 0 mA

Notes: (1) Clamped by input Schottky diodes to GND and V_{CC}

AC Performance Characteristics [1]

(Over guaranteed operating conditions, GND = 0 V)

1. Read Mode:



Parameters	Description	6 ns		5 ns		4 ns		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	6	—	5		4		ns
t_{ACS}	Chip select time	—	4	—	3.5		2.5	ns
t_{ZRCS} [2]	Chip select to HIGH Z	—	5	—	4		3.5	ns
t_{AOS}	Output enable time	—	4	—	3.5		2.5	ns
t_{ZROS} [2]	Output enable to HIGH Z	—	5	—	4		3.5	ns
t_{AA}	Address access time	—	6	—	5		4	ns

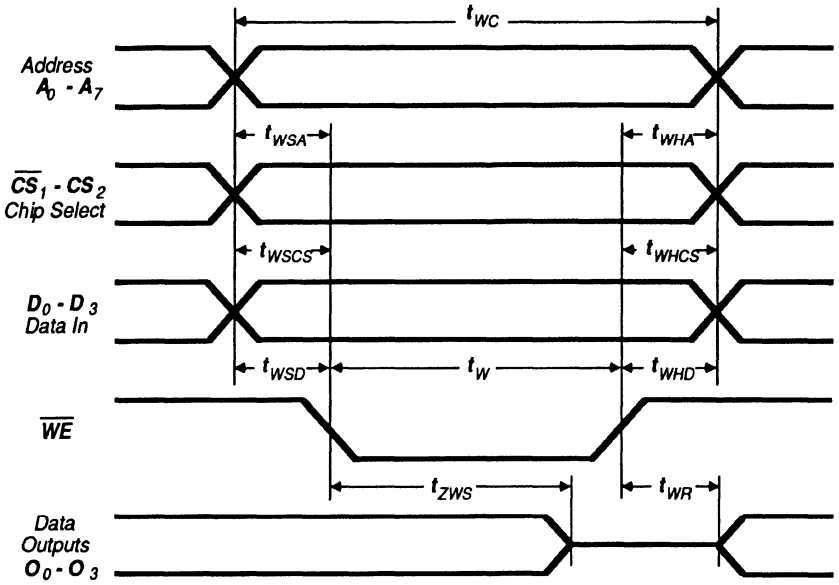
Notes: 1) Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in figure 1 on page 4-5

2) Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in figure 1 on page 4-5

AC Performance Characteristics - continued [1]

(Over guaranteed operating conditions, GND = 0 V)

2. Write Mode:



Paramters	Description	6 ns		5 ns		4ns		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	6	—	5	—	4	—	ns
t_{ZWS} [2]	Write disable to HIGH Z	—	5	—	4	—	3.5	ns
t_{WR}	Write recovery time	—	4.5	—	3.5	—	3	ns
t_W [3]	Write pulse width	4	—	3	—	2.5	—	ns
t_{WSD}	Data setup time prior to write	0	—	0	—	0	—	ns
t_{WHD}	Data hold time after write	2	—	2	—	1.5	—	ns
t_{WSA} [3]	Address setup time	0	—	0	—	0	—	ns
t_{WHA}	Address hold time	2	—	2	—	1.5	—	ns
t_{WSCS}	Chip select setup time	0	—	0	—	0	—	ns
t_{WHCS}	Chip select hold time	2	—	2	—	1.5	—	ns

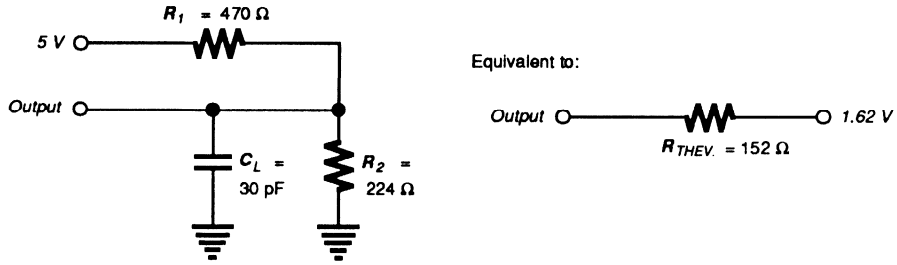
Notes: 1) Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in figure 1 on page 4-5

2) Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in figure 1 on page 4-5

3) t_W measured at t_{WSA} = min; t_{WSA} measured at t_W = min

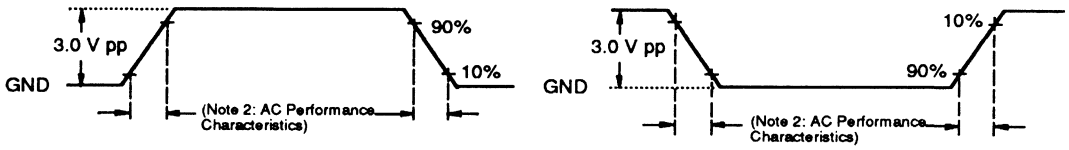
AC Test Loading Condition (Figure 1)

The following conditions apply to the "AC Performance Characteristics" indicated on pages 4-3 and 4-4.



AC Test Input Levels (Figure 2)

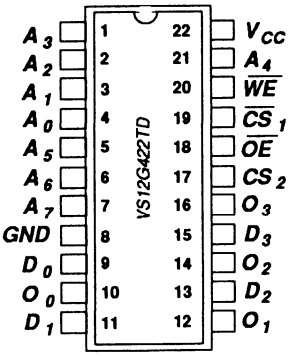
The following conditions apply to the "AC Performance Characteristics" indicated on pages 4-3 and 4-4.



Address Designators

Address Name	*Address Function*	*Pin Number* 22-pin DIP	28-pin LCC
A_0	AX_0	4	21
A_1	AX_1	3	20
A_2	AX_2	2	19
A_3	AX_3	1	17
A_4	AX_4	21	16
A_5	AY_5	5	22
A_6	AY_6	6	23
A_7	AY_7	7	24

Connection Diagram *(22-pin DIP - Top View)*



Pin Description

Pin #	Name	I/O	Description
1-7, 21	A_0 - A_7	I	Address inputs
9, 11, 13, 15	D_0 - D_3	I	Data Inputs
19	$\overline{CS}_1$	I	Chip select input (Active LOW)
10, 12, 14, 16	O_0 - O_3	O	Data outputs
17	CS_2	I	Chip select input (Active HIGH)
20	$\overline{WE}$	I	Write enable input (Active LOW)
18	$\overline{OE}$	I	Output enable input (Active LOW)
22	V_{CC}		5.0 V supply connection
8	GND		Ground connection (0 V)

VS12G478

2K x 2 Self-Timed Static RAM with Purge

Features

- 2048 Words x 2-bit Static RAM, Ideal for Fast Cache or Control Store Applications
- Functionally Compatible with National NM100492 (with the addition of an output latch enable)
- Very Fast: Read/Write Cycle Time 5 or 7 ns (Max)
- Full Chip Bit Purge in 4 Cycles
- 100K ECL Compatible Inputs and Outputs
- Power Dissipation: ≤ 1 W (typical)

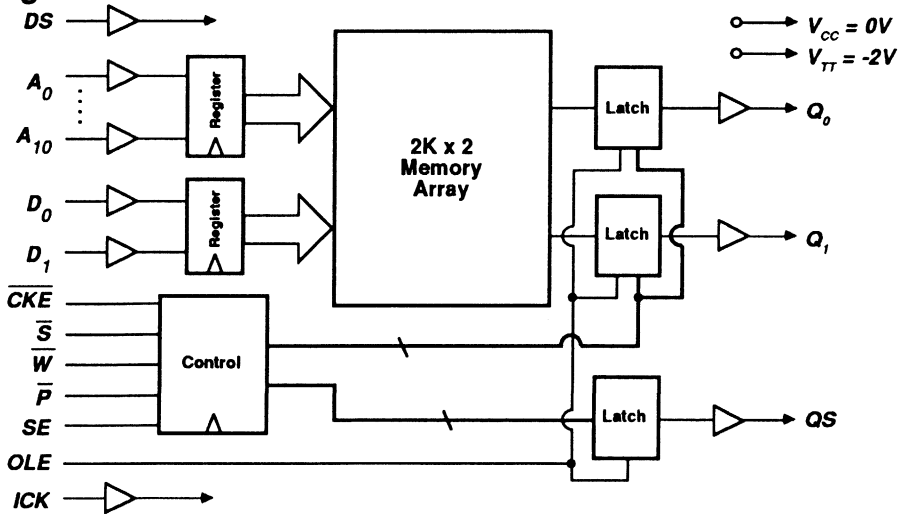
Introduction

The VS12G478 is a high speed, fully decoded 4096-bit read write self-timed static random access memory organized as 2048 words by 2 bits. This RAM is intended for use in high speed ECL computer applications such as register files, writable control stores, cache RAMs, cache tag RAMs, and addressable translation lookaside buffers. This device is I/O compatible with standard F100K ECL logic, allowing trouble free interfacing in high performance ECL systems. Operation is from a standard -2.0 Volt power supply, and all inputs are registered and all outputs are latched.

The SRAM features a 4 cycle "clear-all-bits-to-zero" purge function. The purge function is especially useful in multitasking systems with cache tags which require a validity bit purge in a very short time. On-chip circuitry creates an internal write pulse intended to ease system timing. A diagnostic serial scan mode is also supported. The scan function allows examination and modification of internal register states.

The VS12G478 is available with a 5 or 7 ns worst case cycle time, and either a read or a write operation can be performed in one cycle. Total power dissipation is less than 1 W, and the chip is packaged in a 28-pin leaded ceramic chip carrier. The VS12G478 is fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation.

Block Diagram



Truth Tables

Normal Operation: *SE Low for Current and Previous Cycle*

Inputs						Output	Description
$\overline{CKE}$	$\overline{P}$	$\overline{S}$	$\overline{W}$	AN	DN	Q	
H	X	X	X	X	X	NC	No operation
L	L	X	X	X	X	L	PURGE*
L	H	H	H	X	X	L	Deselect (READ)
L	H	L	H	V	X	V	READ
L	H	H	L	X	X	NC	WRITE inhibit
L	H	L	L	V	V	NC	WRITE (Hidden), outputs remain held during write.

** PURGE starts a 4 cycle RAM clear operation. During the next 4 cycles, all other inputs except SE are ignored.*

Scan Mode Operation:

Inputs				Outputs		Description
Prior SE	Current SE	Registered $\overline{CKE}$	DS	Q	QS	
L	L	X	X	X	DI	Normal operation
L	H	X	V	NC	DO	Enter SCAN, do first shift. DS scanned in.
H	H	X	V	NC	V	SCAN mode
H	L	L	V	L/V/NC	V	Exit SCAN. Shift, then perform Scanned Instruction*
H	L	H	V	V	V	Exit SCAN, NOP. Update Output Latches to Scanned In Values

** If PURGE instruction is scanned in, then the PURGE will start at the scanned in purge machine state.*

Absolute Maximum Ratings (1)

Power Supply Voltage, V_{TT} potential to GND ..... -2.5V to +0.5V
Input Voltage Applied, V_{IN} (2) ..... +0.5V to V_{TT}
Output Current, I_{OUT}, (DC, output HIGH) ..... -50 mA
Maximum Junction Temperature, T_j ..... 150°C
Case Temperature Under Bias, T_C ..... -55°C to +125°C
Storage Temperature, T_{STG} (3) ..... -65°C to +150°C

Recommended Operating Conditions

Supply Voltage, V_{TT} ..... -2.0V ± 5%
Operating Temperature Range, T (3) ..... 0° to 70°C

Notes: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) V_{TT} must be applied before any input signal voltage (V_{IN}) and V_{IN} must be greater than V_{TT} - 0.5V.

(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

DC Characteristics

ECL Inputs/Outputs:

(Over recommended operating conditions with external V_{REF}[1]. $V_{CC} = V_{CCA} = GND$, Output load 50Ω to V_{TT}.)

Parameter	Description	Min	Max	Units	Conditions
V_{IH}	Input HIGH Voltage	-1140	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW Voltage	-2000	-1500	mV	Guaranteed LOW for all inputs
V_{OH}	Output HIGH Voltage	-1020	-700	mV	Output load = 50 Ω to -2 V
V_{OL}	Output LOW Voltage	-2000	-1620	mV	Output load = 50 Ω to -2 V
I_{IH}	Input HIGH Current	—	+200	µA	$V_{IN} = V_{IH}$max
I_{IL}	Input LOW Current	-50	—	µA	$V_{IN} = V_{IL}$max
I_{IHP}	Input Pulldown Current ($\overline{CKE}$, CS, SE, DS)	0	+500	µA	

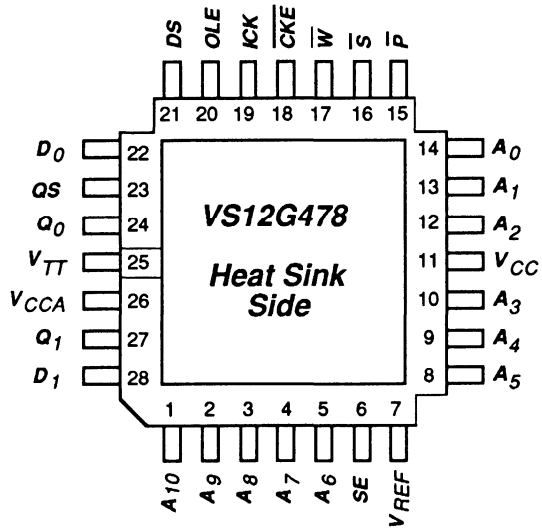
Note: (1) External reference = -1.32V ± 25 mV.

4

Power Dissipation: *(Over recommended operating conditions, V_{CC} = GND, outputs open circuit.)*

Parameter	Description	Min	Max	Units	Conditions
I_{TT}	Power Supply Current	-500	—	mA	T_{CYCLE} = 5 ns
P_D	Power Dissipation	—	1.05	W	T_{CYCLE} = 5 ns

Pin Description



Address Designators

Address Name	Address Function
A_0	X_0
A_1	X_2
A_2	X_1
A_3	X_3
A_4	X_5
A_5	X_4
A_6	Y_0
A_7	Y_2
A_8	Y_1
A_9	Y_3
A_{10}	Y_4

Name	I/O	Description
A_0 - A_{10}	I	Address inputs used to select the memory locations for storing or retrieving data.
D_0, D_1	I	Data inputs stored in the specified address location during a write operation.
$\overline{CKE}$	I	Clock Enable input. Allows normal operation when LOW. Holds outputs and disables writes and purges when HIGH. Upon exiting SCAN mode, causes chip to either execute scanned-in instruction ($\overline{CKE}$ LOW), or transfer scan contents to outputs and do a no-op ($\overline{CKE}$ HIGH).
$\overline{P}$	I	Purge input. Clocking in a LOW input will start a 4 cycle reset of all bits in the RAM. During the purge operation all inputs except Scan Enable are ignored. Outputs are disabled for the duration of the purge.
$\overline{S}$	I	Chip Select input. When active (LOW) allows normal read and write cycles to occur. When inactive, and when Write Enable is also inactive, a de-selected read operation will disable the outputs. Writes are disabled when the chip is de-selected.
$\overline{W}$	I	Write Enable input. When active (LOW), causes a write operation to occur. Outputs are held in previous state during writes.
ICK	I	Input Clock. All inputs except OLE are registered on the rising edge of ICK.
OLE	I	Output Latch Enable. HIGH transparent latch enable signal to the output latches.
DS	I	Serial Data input. Scan shift register input.
SE	I	Scan Enable input. Enables the serial scan diagnostics mode. During all cycles when this pin is active (HIGH) the scan registers shift once. Writes and purges are disabled and the Data Outputs are held.
Q_0, Q_1	O	Data Outputs. Latched RAM data outputs.
QS	O	Serial Data Output. Scan data output.
V_{TT}		Negative supply (-2V).
V_{CC}		Positive supply (GND).
V_{CCA}		Positive supply (GND) for output buffers only.
V_{REF}		ECL reference level input when not using internally generated reference level.

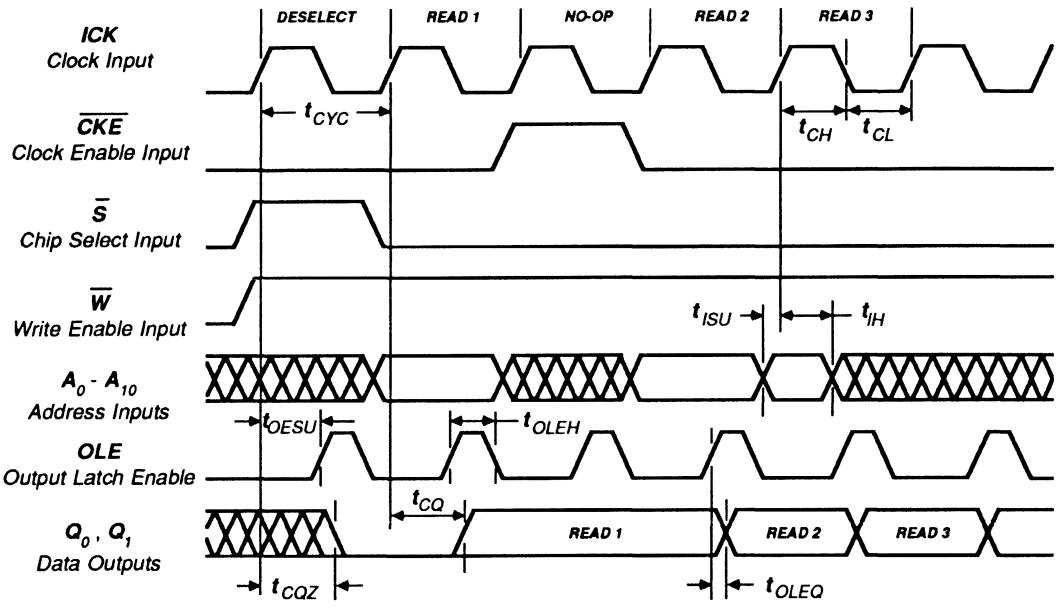
AC Performance Characteristics:

(Over recommended operating conditions, $V_{CC} = V_{CCA} = GND$)

1. Read Mode:

A read cycle is performed when the following conditions are present at the rising edge of ***ICK:*** $\overline{CKE}$ = LOW, $\overline{S}$ = LOW, $\overline{W}$ = HIGH, ***SE*** = LOW and was LOW for the previous cycle, $\overline{P}$ = HIGH and no purge in progress. (i.e. $\overline{P}$ has been high for the previous 4 cycles and Scan Mode was not exited into a purge that is still in progress.)

Read Mode Waveforms



Parameter	Description	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{CQ}	Access Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{CQZ}	Disable Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{ISU}	Input Setup Time	500	—	500	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{CH}	Clock HIGH Time	1.5		2.0	—	ns	
t_{CL}	Clock LOW Time	1.5	—	2.0	—	ns	
t_{OLEQ}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$
t_{OLEH}	Output Latch Pulse Width	1.0	—	1.5	—	ns	
t_{OESU}	Output Latch Set-up Time	3.0	—	4.5	—	ns	

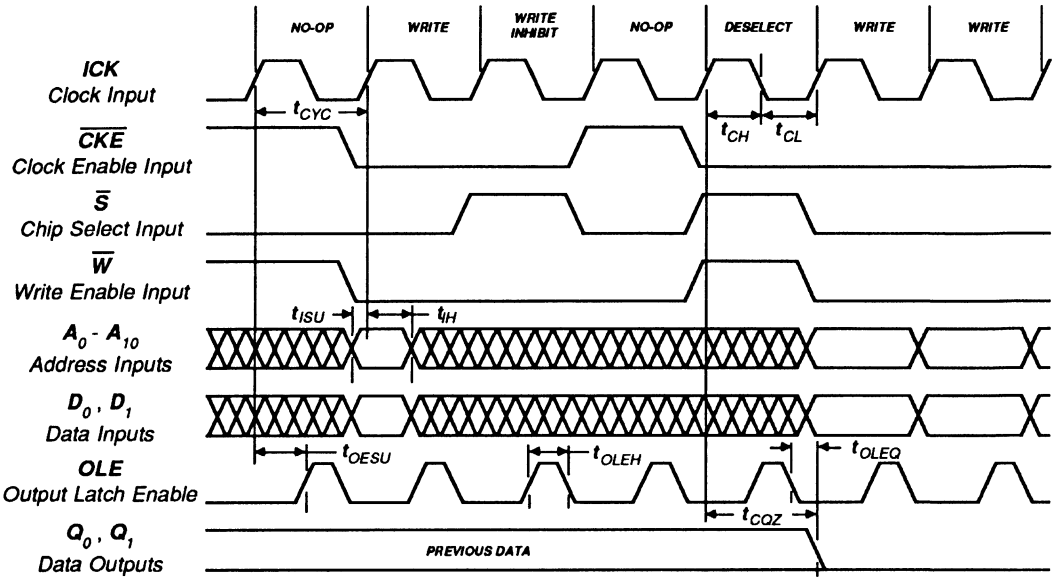
AC Performance Characteristics *(continued)*

(Over recommended operating conditions, V_{CC} = V_{CCA} = GND)

2. Write Mode:

A write cycle is performed when the following conditions are present at the rising edge of ***ICK:*** $\overline{CKE}$ = LOW, $\overline{S}$ = LOW, $\overline{W}$ = LOW, ***SE*** = LOW and was LOW for the previous cycle, $\overline{P}$ = HIGH and no purge in progress. (i.e. $\overline{P}$ has been high for the previous 4 cycles and Scan Mode was not exited into a purge that is still in progress.)

Write Mode Waveforms



Symbol	Parameter	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{CQZ}	Disable Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{ISU}	Input Setup Time	500	—	500	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{CH}	Clock HIGH Time	1.5	—	2.0	—	ns	
t_{CL}	Clock LOW Time	1.5	—	2.0	—	ns	
t_{OLEQ}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$
t_{OLEH}	Output Latch Pulse Width	1.0	—	1.5	—	ns	
t_{OESU}	Output Latch Set-up Time	3.0	—	4.5	—	ns	

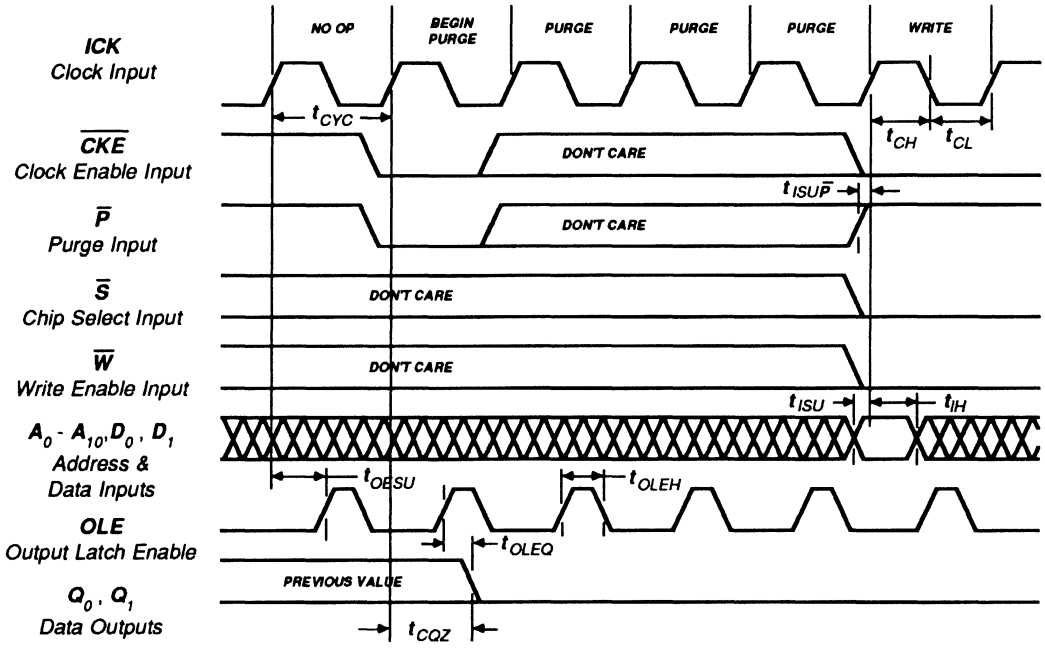
AC Performance Characteristics *(continued)*

(Over recommended operating conditions, V_{CC} = V_{CCA} = GND)

3. Purge Mode:

A full chip reset begins when the following conditions are present at the rising edge of ***ICK***: ***$\overline{CKE}$*** = LOW, ***SE*** = LOW and was LOW for the previous cycle, ***$\overline{P}$*** = LOW. Once started, the purge cycle takes 4 cycles to complete. During this time, all inputs except SE are ignored and outputs are disabled.

Purge Mode Waveforms



Parameter	Description	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{CQZ}	Disable Time	2.0	5.0	2.0	7.0	ns	Output Latch Transparent
t_{ISU}	Input Setup Time (except $\overline{P}$)	500	—	500	—	ps	
$t_{ISU\overline{P}}$	Purge Input Setup Time	750	—	750	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{CH}	Clock HIGH Time	1.5		2.0	—	ns	
t_{CL}	Clock LOW Time	1.5	—	2.0	—	ns	
t_{OLEQ}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$
t_{OLEH}	Output Latch Pulse Width	1.0	—	1.5	—	ns	
t_{OESU}	Output Latch Set-up Time	3.0	—	4.5	—	ns	

4. Scan Mode:

Scan Mode is entered when ***SE*** is brought high. When in Scan Mode, the input registers are reconfigured as shift registers and each rising edge of ***ICK*** causes them to shift. The state of ***DS*** is shifted in and the state of ***QS*** is updated. ***QS*** is latched by ***OLE*** like the regular outputs. While ***SE*** is high, Writes to the array are disabled and the outputs are held. On the first clock cycle when ***SE*** is brought low, the rising edge of ***ICK*** causes the registers to shift and conditionally execute the scanned in instruction. If the scanned in $\overline{CKE}$ is low, the instruction executes with normal timing; if $\overline{CKE}$ is high, the outputs update to the values scanned into the Q scan bits and the RAM performs a 'NO-OP'. If a purge machine cycle number other than zero is scanned in, however, the outputs will be disabled and purge will continue regardless of the state of $\overline{CKE}$. Note: If a purge state other than zero is scanned in, the $\overline{P}$ register should be scanned in to a zero.

The purge state machine consists of 3 bits; a registered $\overline{P}$ signal and a 2 bit counter. Purge will begin anytime the $\overline{P}$ register is LOW and the $\overline{CKE}$ register is LOW. On the next ***ICK*** rising edge, the counter will increment to 1 and all inputs except ***SE*** will be ignored until the counter wraps around to 0 again. If a non-zero value is scanned into the purge state machine (which is included in the scan loop) then the purge will continue from that point on exit from Scan Mode regardless of the state of $\overline{CKE}$. The scan sequence is input ***DS,*** to ***Q0, D0*** $\overline{CKE}$, $\overline{W}$, $\overline{S}$, $\overline{P}$, *PURGE LSB, PURGE MSB,* ***A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, D1, Q1,*** to ***QS*** out.

Parameter	Description	VS12G478-5		VS12G478-7		Units	Conditions
		Min	Max	Min	Max		
t_{CYC}	Cycle Time	5.0	—	7.0	—	ns	
t_{ISU}	Input Setup Time	500	—	500	—	ps	
t_{IH}	Input Hold Time	1.0	—	1.5	—	ns	
t_{OLEQS}	Output Latch Enable Time	1.0	2.0	1.0	2.5	ns	$t_{OLE} - t_{ICK} > t_{OESU}$

FOUNDRY SERVICES

H-GaAs II Enhancement/Depletion MESFET Process

Features

- Enhancement/depletion GaAs process
- VLSI complexity
- Self-aligned active devices
- 0.6 micron effective gate length
- 4 inch diameter GaAs wafers
- Sub-100 ps gate delays
- Five interconnect levels
- Extended temperature range operation
- Radiation resistant
- Mil 883C processing

GaAs Advantages

Gallium arsenide is the clear IC technology choice where either speed alone or speed and power are the critical design parameters. GaAs derives its superiority from a variety of factors, including a high electron mobility which results in very fast MESFETs, and an inherent hardness to ionizing radiation. To these, enhancement/depletion (E/D) mode technology adds compatibility with logic families which require relatively small numbers of active devices per function implemented.

GaAs E/D technology allows the designer the flexibility of implementing a variety of logic families, including the ones available in D-mode technology. Some of the well known families open to use in E/D GaAs are Direct-Coupled FET logic (DCFL), Source-coupled FET logic (SCFL), Buffered Direct-Coupled FET logic (BDCFL), Buffered FET logic (BFL) and Schottky diode FET logic (SFL). Each family has unique power dissipation, gate delay, and load drive characteristics. Any and all of these logic families can be mixed in the same circuit to optimize performance.

The H-GaAs II Process

Vitesse offers a third generation NMOS-like, planar process for the fabrication of digital and mixed analog-digital integrated circuits. H-GaAs II is a scaled version of the process first implemented by Vitesse in 1986. The high yield and manufacturability of this approach has been established through volume shipment of VLSI complexity circuits for use in a wide array of applications.

The H-GaAs II process employs up to five levels of metallization requiring as little as thirteen mask levels to produce self-aligned MESFETs and diodes. The process has been specifically designed for the implementation of VLSI circuits with over one million active devices. H-GaAs II is currently used by Vitesse to implement standard and semi-custom products including the FURY Series of gate arrays, proprietary high performance processor chip sets, and static RAMs.

The use of a tungsten-based refractory metal for gates and local interconnects ensures stability during high temperature processing. As in VLSI silicon processing, an aluminum alloy is used for the four levels of global interconnects. Dry etching of metals and dielectrics is used throughout in order to maximize yields.

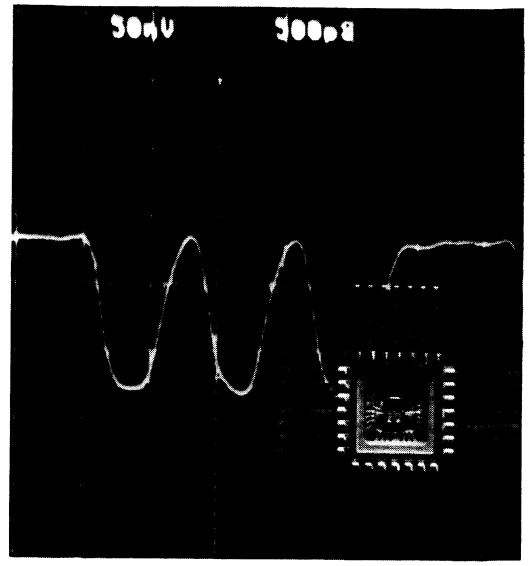
H-GaAs II Metal Pitches

METAL	LINE WIDTH	SPACING
Gate	0.8	1.5
Metal 1	1.5	2.0
Metal 2	2.0	2.0
Metal 3	3.0	3.0
Metal 4	Unpatterned	

Quality Assurance

Quality control mechanisms are built into every step of Vitesse's fabrication process, from wafer acquisition to final testing. These mechanisms, like the models and design tools, are continually refined through use in the production of Vitesse's standard products.

The assurance of the quality of finished wafers begins before the wafers are received at Vitesse's facility. Four inch diameter semi-insulating GaAs wafers are used exclusively for H-GaAs II processing. Careful screening has already reduced the number of vendors from which Vitesse acquires its wafers to a relative few. These suppliers have been provided with a proprietary set of requirements specifying how Vitesse's wafers must be prepared, cleaned, tested, and packaged for our use.



The Vtesse process can be used to implement circuits which operate at clock rates well above 1 GHz. The 4:1 multiplexer shown above uses SCFL circuitry and operates at 2.5 Gb/s.

SCFL

MACRO	DELAY	DELAY/ F.O.	WIRE DELAY	P_D
Inverter	140ps	15ps	70ps/mm	23mW
D Flip-flop	230ps	15ps	70ps/mm	45mW
2:1 Mux Select→ Output	160ps	15ps	70ps/mm	23mW

DCFL

FUNCTION	DELAY	DELAY/ F.O.	WIRE DELAY	P_D
Inverter	90ps	13ps	80ps/mm	1.0mW
D Flip-flop	400ps	13ps	80ps/mm	3.9mW
2:1 Mux Select→ Output	300ps	13ps	80ps/mm	2.1mW

The parameters shown above are provided as a quick reference to the performance of two commonly used logic families implemented using Vitesse's proprietary process. The data reflects the fact that the choice of logic depends heavily on the circuit — or portion of a circuit — being produced (more than one logic type may be mixed in a given design).

The parameters given above are based on worst case characteristics, and 70° C operation. All of the delay values assume unit fan-out and no metal loading. All D-mode devices were used to implement the two level series gated SCFL example. The nominal supply voltage for SCFL is -5.2V. Both E-mode and D-mode devices were employed to implement the DCFL circuits. The nominal supply voltage for DCFL is -2V.

**HSPICE is a product of Meta-Software*

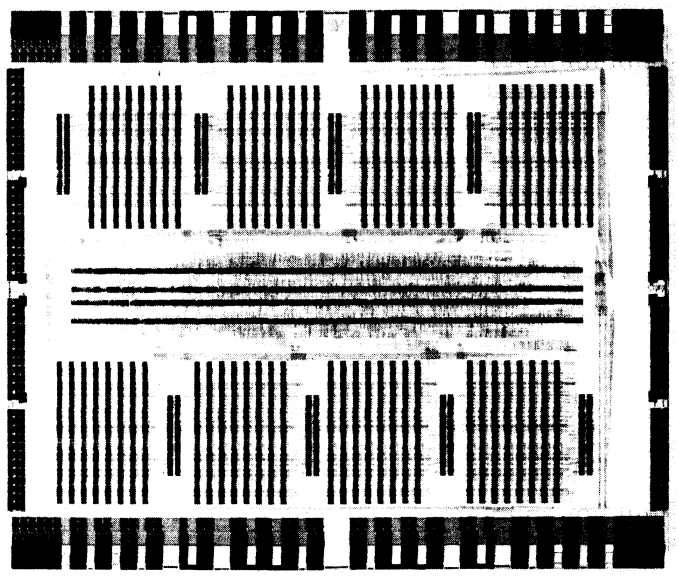
Wafers in process are inspected at 33 points, tested in processing, and tested again after final passivation.

The H-GaAs process currently uses 5x steppers with a maximum reticle size of 13mm x 13mm. Each reticle contains a process control monitor (PCM) for use in parametric screening and quality control. At each of the metallization steps, the devices within the PCM are inspected and measured. In addition to other parameters, transistor quality, transistor-to-transistor variation, and metal connections (shorts/opens) are checked.

Final results of the measurement of PCMs at various positions on the wafer determine whether a wafer will be released to the customer. The results of the PCM measurements are released to the customer with the wafers.

Customer Support

Vitesse offers the designer an array of design tools and support services developed specifically for custom designs. These tools and services have been assembled to provide a designer with a high degree of confidence to implement high performance circuits which will



Photomicrograph of a 22K gate chip implemented in H-GaAs II

function correctly the first time.

Before any instruction or design has begun, a joint review of the customer's requirements is performed and a Vitesse project manager is assigned to support and track each foundry program. This project manager is provided to insure timely response to a customer's needs during the program and to report the status of the customer's wafers at any time during the fabrication cycle.

The Vitesse Foundry Design Manual, a proprietary publication which is released to the customer on a non-disclosure basis, provides a road map through the design and fabrication process. This manual, when combined with the design training course offered by Vitesse, provides a comprehensive method by which designers can familiarize themselves with the proces, rules, aids, and tools, as well as specific examples of Vitesse's digital GaAs IC design process.

The guide provides complete instructions for designing custom cells compatible with the Vitesse standard cell library. In addition, it contains information on testing and packaging, including test vector formats and assembly/build diagrams for the entire line of Vitesse high-speed packages.

Vitesse supports the HSPICE* circuit simulator for use in full custom design projects. HSPICE is one of the most popular commercially available simulators and is characterized by excellent convergence and pre- and post-processing facilities. Vitesse, in conjunction with Meta-Software, has developed a model which accurately reflects the characteristics of MESFETs fabricated in the H-GaAs II process. The temperature dependent model includes backgating, short and narrow channel effects, and velocity saturation.

Parameter files that represent device performance shifts due to process variations are supplied by Vitesse for use with the HSPICE simulator. With the aid of HSPICE, the designer can simulate circuit performance over all process corners, thereby simplifying performance/yield trade-offs.

Several other software tools are also provided, including ECAD-compatible files for physical layout design rule checking, electrical design rule checking, and layout-vs-schematic checking.

Design consultation with Vitesse senior circuit designers is included as part of the standard foundry program package, and an optional classroom course is offered for in-depth

review of the design, testing, and pack-aging of VLSI GaAs circuits. Use of Vitesse's design center is also optionally available. Final design results can be submitted in the form of GDS II or CIF-format tapes.

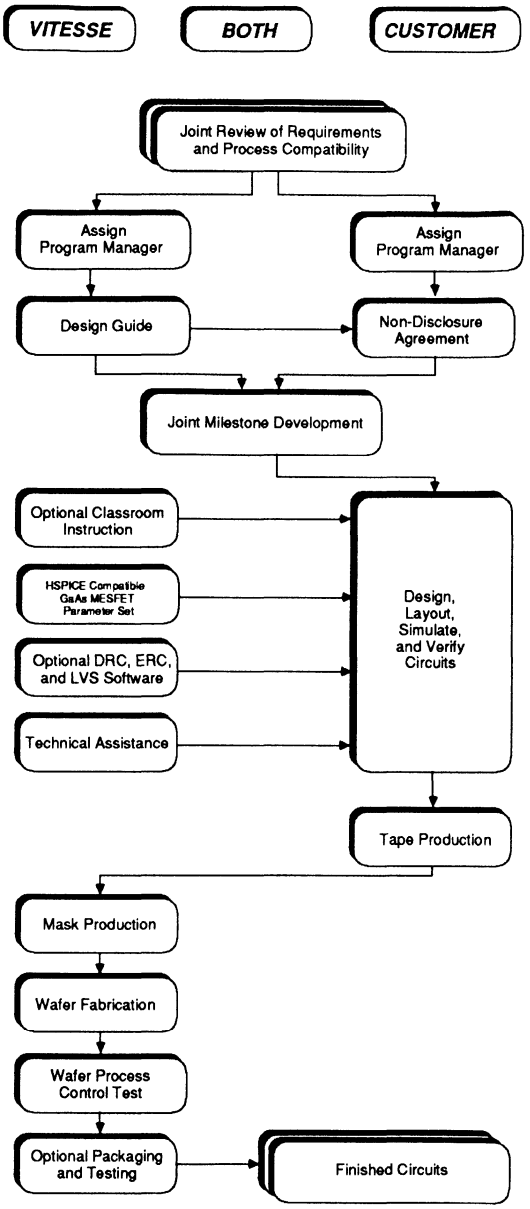
Optional Services

Assembly and testing are provided as customer options. This includes functional and critical path testing at both the wafer and for level packaged parts. Vitesse has a full complement of IC test equipment including a Teradyne J953 high pin count tester and Teradyne J386 memory tester. The J953 can accommodate up to 256 I/O signals with a maximum data rate of 50MHz. The edge placement accuracy on both inputs and outputs is ± 250psec. The J386 has an algorithmic pattern generator for the generation of regular bit patterns. That system is capable of functional pattern generation at a maximum rate of 100MHz, and has an input signal rise/fall time of under 400ps. AC parameters for the tester include a 1GHz bandwidth, 50ps resolution, and 200ps measurement accuracy. More detailed specifications of its capabilities are available upon request.

Assembly and packaging services are available. Ceramic chip carriers, DIPs, and pin grid arrays capable of supporting edge rates of 150ps are the standard package forms; custom package development will be considered as a special quote. Vitesse can provide Mil 883 compliant chips to customer specifications.

Turnaround

In a typical IC development program most of the time is spent on design and layout, which is the responsibility of the customer. The primary goal of Vitesse's consulting services and software tools is to minimize that portion of the schedule. Once the design and layout are complete, the time from mask procurement to tested wafers usually requires 6 to 7 weeks. This includes 1 week for mask making, three to four weeks for fabrication and two weeks for assembly and test.



Package Outlines

Introduction

This section contains the outlines for all of the standard packages currently offered by Vitesse. All are cavity down, multilayer ceramic packages with Cu-W heat spreaders for efficient cooling. The only exceptions being the plastic 28-pin J-lead MQUAD™ and the 132-pin MQUAD which are both low cost, high volume packages. This arrangement results in controlled impedance on signals, good cross talk control, low impedance power supply leads and low thermal resistance from junction to case.

In most ASIC designs, the size of the die and package are dictated by the number of signal I/O and/or equivalent gates. Table 1 summarizes the standard packages with the corresponding die size and maximum signal I/O that can be accomodated. Vitesse has custom package development and complete assembly facilities. New packages can be developed or die can be assembled in non-Vitesse packages. New packages may be currently under development based on new standard products and customer designs. If none of the packages listed in the table meet your requirements, contact Vitesse for the latest information on package availability.

Table 2 summarizes Vitesse's standard products and the packages which are available for each. Also listed is the page on which the package drawing appears.

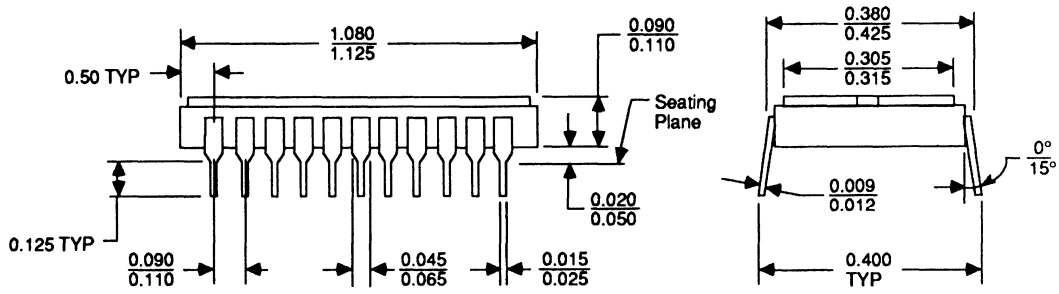
Table 1: *Vitesse Standard Packages*

Package	***Number of I/O (Max. Outputs)***	***Die Size (μm)***
22 pin Ceramic DIP	20	2160 x 2450 2880 x 2450
24 pin Ceramic DIP	22	2880 x 2450 4325 x 3675
28 pin LDCC or LCC	26	2160 x 2450 2880 x 2450
52 pin LDCC, LCC,or J-lead MQUAD	41	2880 x 3675 4325 x 3675
132 pin LDCC or MQUAD	92	3440 x 5540
149 pin PGA	120	4325 x 7350
164 pin LDCC	120	4325 x 7350
211 pin PGA	174	8650 x 7350
256 pin LDCC	196	8650 x 7350
344 pin LDCC	256	13780 x 7730

Table 2: Product vs. Package Summary

Product	Description	Packages	Page
VS8001 VS8002	12:1 Multiplexer/1:12 Demultiplexer Chip Set	52 pin Ceramic LDCC or LCC	6-6
VS8004 VS8005	4:1 Multiplexer/1:4 Demultiplexer Chip Set (2.5 Gb/s)	28 pin Ceramic LDCC or LCC	6-4
VS8010 VS8011 VS8012	SONET - High Speed 8 Bit Mux/Demux Products	52 pin Ceramic LDCC or LCC	6-6
VS8021 VS8022	SONET - 2.5 Gb/s Chip Set 8-Bit Mux/Demux	52 pin Ceramic LDCC or LCC	6-6
VS12G422T	256 x 4 Static RAM (TTL)	22 pin Ceramic DIP	6-3
VS12G478	2K x 2K Self-Timed Static RAM with Purge	28 pin Ceramic LDCC	6-4
VSC1500	HS Series, 1500 Gate Structured Cell Array (1.5GHz)	52 pin Ceramic LDCC or LCC	6-6
VSC1520	HS Series, 1500 Gate Structured Cell Array (2.5GHz)	52 pin Ceramic LDCC or LCC	6-6
VSC864	64 x 64 Crosspoint Switch	344 pin Ceramic LDCC	6-17
VSC2000	LP Series, 2000 Gate Array	52 pin Ceramic LDCC or LCC	6-6
VSC4500	LP Series, 4000 Gate Array	149 pin Ceramic PGA 164 pin Ceramic LDCC or LCC	6-9 6-11
VSC3K	FURY Series, 3500 Gate Array	132 pin Ceramic LDCC	6-7
VSC5K	FURY Series, 6400 Gate Array	149 pin Ceramic PGA 164 pin Ceramic LDCC or LCC	6-10 6-12
VSC10K	FURY Series, 13000 Gate Array	211 pin Ceramic PGA 256 pin Ceramic LDCC	6-14 6-15
VSC15K	FURY Series, 17000 Gate Array	211 pin Ceramic PGA 256 pin Ceramic LDCC	6-14 6-15
PLR2KT	FURY Series, 30,000 Gate Array	344 pin Ceramic LDCC	6-17

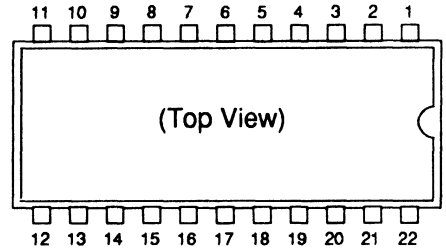
22 Pin Ceramic DIP



22-pin leaded (400 mil) sidebraze dual in-line package

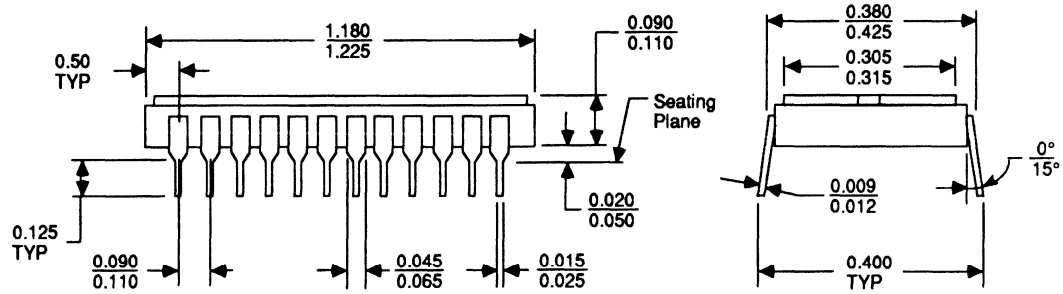
22 Ceramic DIP Pin Functions

PIN	FUNCTION
1-7	Input/Output
8	— Supply
9-21	Input/Output
22	+ Supply



6

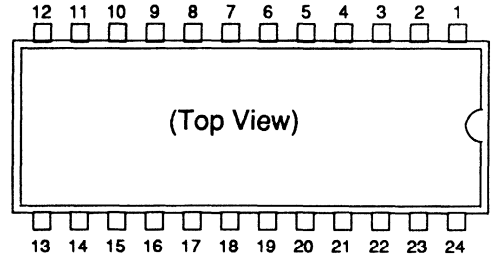
24 Pin Ceramic DIP



24-pin leaded (400 mil) sidebraze dual in-line package

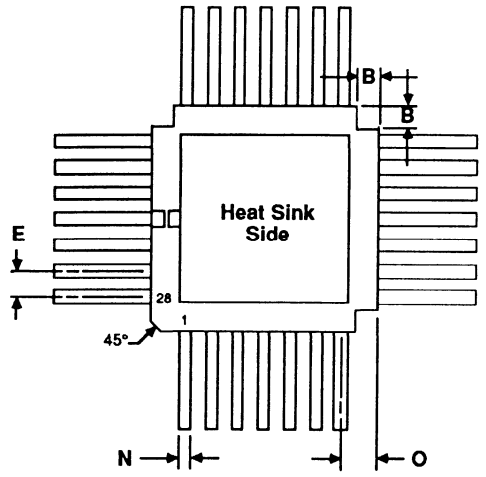
24 Ceramic DIP Pin Functions

PIN	FUNCTION
1-5	Input/Output
6	+ Supply
7	Extra Supply or I/O
8-17	Input/Output
18	— Supply
19-24	Input/Output

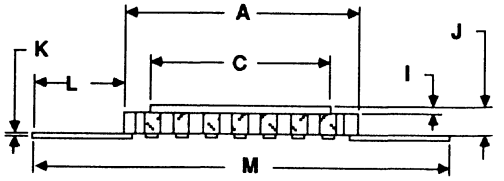


NOTES: 1) Drawings not to scale.
2) All dimensions given in inches.
3) Max. and min. tolerance are indicated.
4) Package: Ceramic (alumina); Heat sink: Copper-tungsten; Leads: Alloy 42 with gold plating.

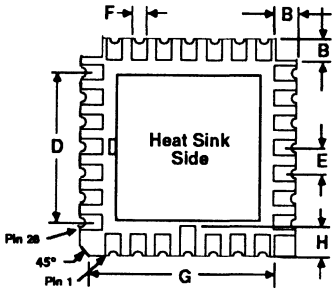
28 Pin Leaded and Leadless Ceramic Packages



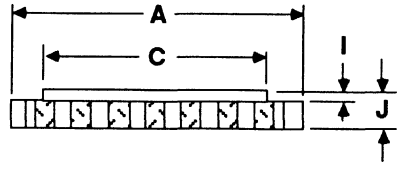
28-Pin Leaded Ceramic Package (LDCC)



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	11.176/11.682	0.440/0.460	I	0.406/0.610	0.016/0.024
B	1.016/1.524	0.040/0.060	J	1.715/2.223	0.075/0.095
C	9.652/10.160	0.300 TYP	K	0.090/0.242	0.004/0.008
D	7.493/7.747	0.300 TYP	L	5.842/6.858	0.230/0.270
E	1.143/1.397	0.050 TYP	M	22.860/25.398	0.900/1.000
F	0.762/1.016	0.035 TYP	N	0.356/0.559	0.014/0.022
G	9.271	0.365	O	1.525/2.287	0.075 TYP
H	1.778	0.070			



28 Pin Leadless Ceramic Package (LCC)

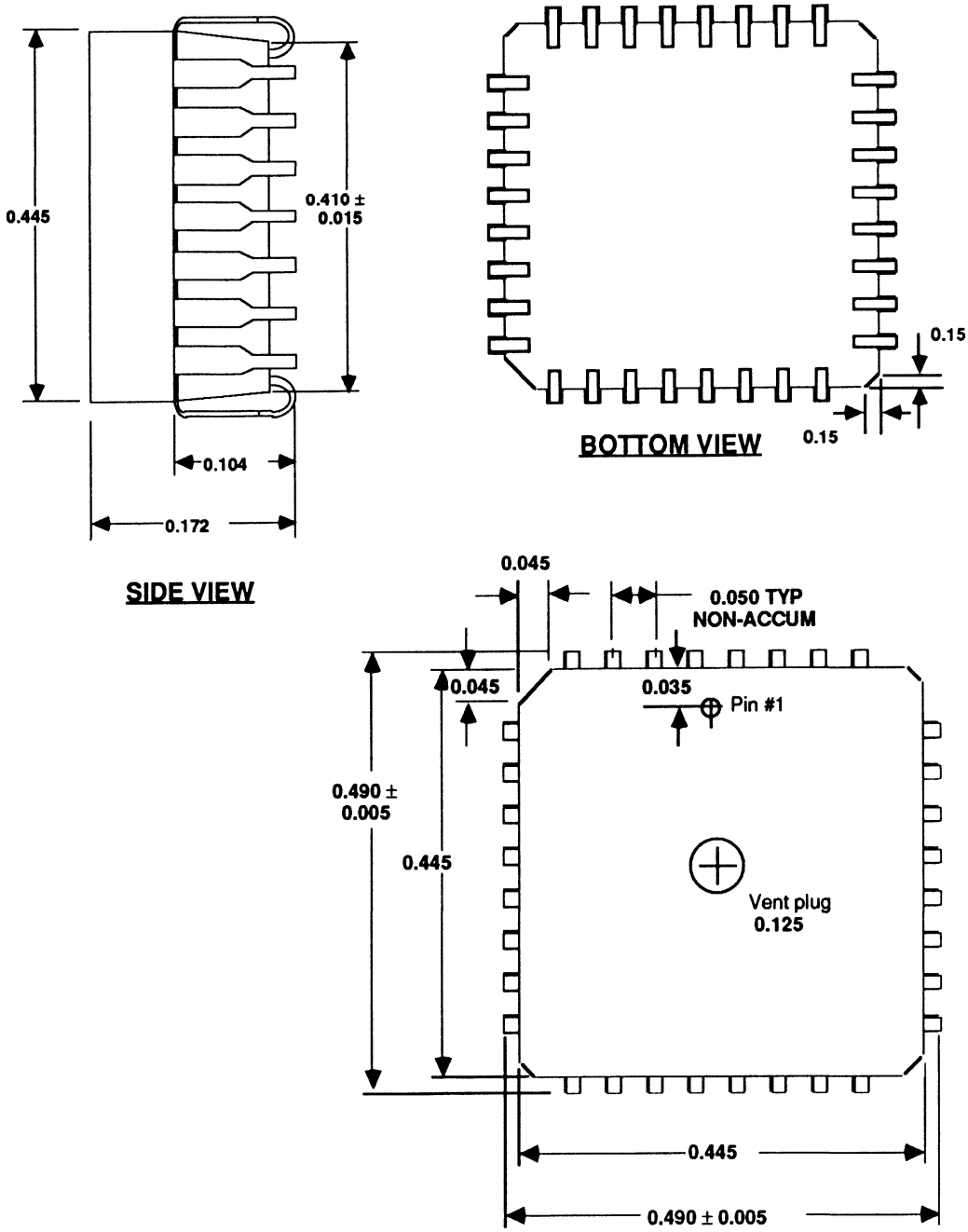


28 LDCC or LCC Pin Functions

PIN	FUNCTION	PIN	FUNCTION
1-3	Input/Output	18	Supply or I/O
4	Supply or I/O	19-24	Input/Output
5-10	Input/Output	25	- Supply (Substrate)
11	Supply or I/O	26-28	Input/Output
12-17	Input/Output		

NOTES: 1) Drawings are not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

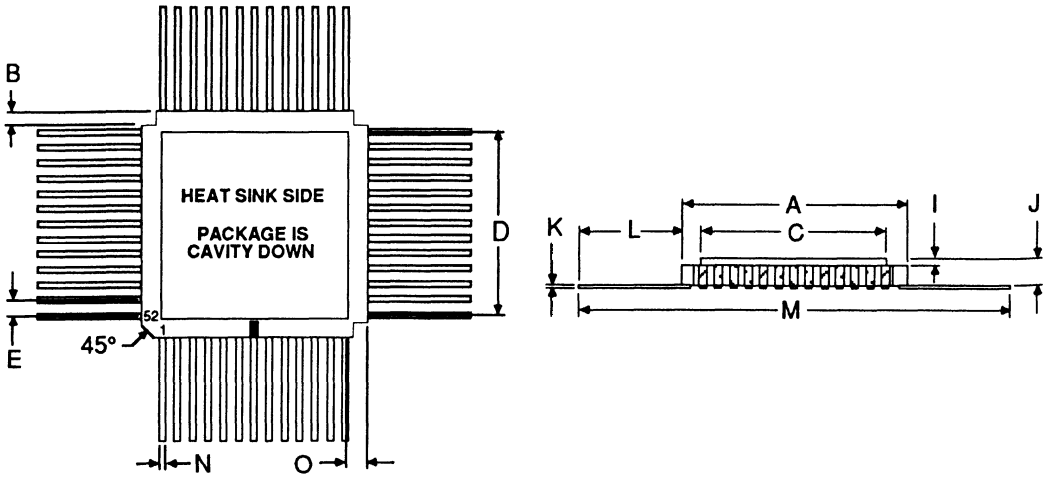
28 Pin J-Lead MQUAD™ Package



Notes:

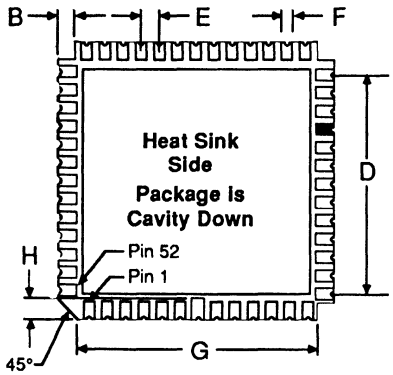
1) All non-toleranced dimensions are shown at nominal.
2) All dimensions in inches.
3) Drawing not to scale.
3) Package is black annodized Aluminum. Leads are copper alloy.

52 Pin Leaded and Leadless Ceramic Packages

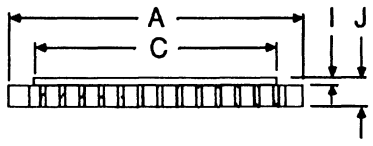


Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	18.54/19.56	0.730/0.770	I	0.41/0.61	0.016/0.024
B	1.02/1.52	0.040/0.060	J	2.03/2.79	0.080/0.110
C*	15.49/16.51	0.610/0.650	K*	0.09/0.24	0.003/0.009
D*	15.24 TYP	0.600 TYP	L	4.83/5.08	0.190/0.200
E	1.27 TYP	0.050 TYP	M	29.46 TYP	1.160 TYP
F	0.76/1.02	0.030/0.040	N	0.36/0.56	0.014/0.022
G	16.94 TYP	0.667 TYP	O	1.75/1.90	0.069/0.075
H	1.91/2.41	0.075/0.095			

* At package body.



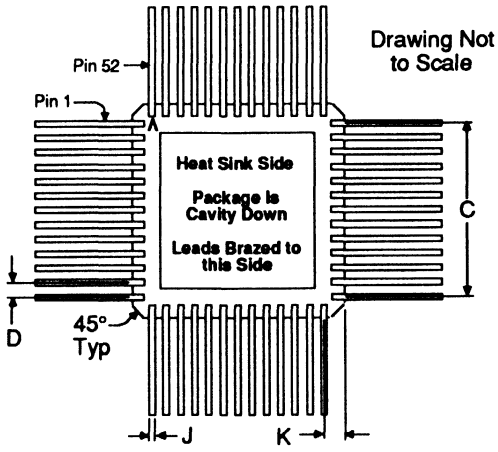
52 Pin Leadless Ceramic Package (LCC)



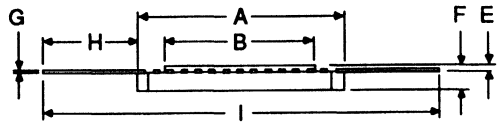
Notes: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

Pin	Function	Pin	Function
1-3, 5-6, 8-9, 11-17	Input/Output	4,10,18,30,36,43,49	GND
19-22, 24-29, 31-32	Input/Output	7,46	(-) Supply 1
34-35, 37-42, 44-45	Input/Output	33	Supply 2
47-48, 50-52	Input/Output	23	(substrate)

52 Pin Leaded Package (for FURY VSC3K only)



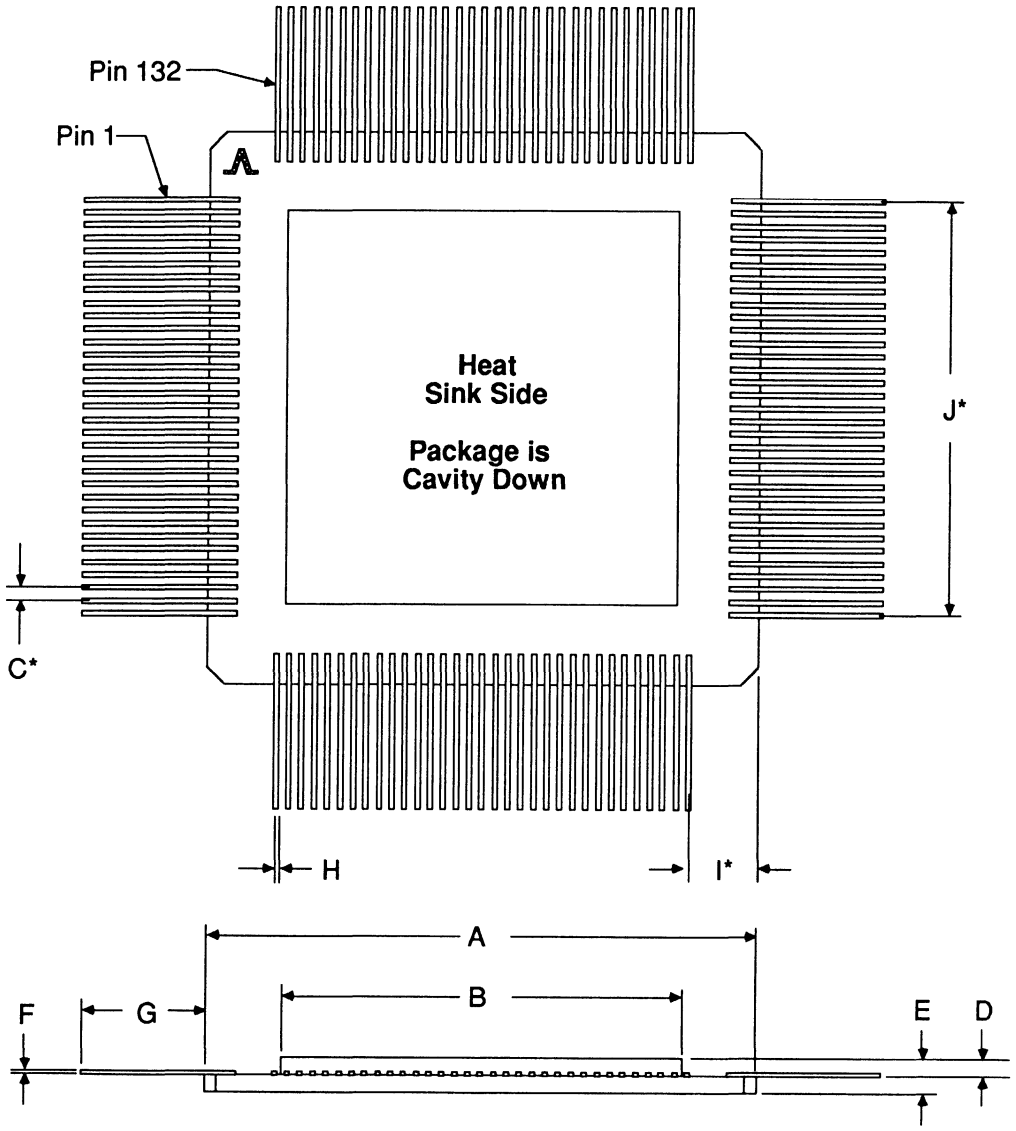
52 Pin Leaded Ceramic Package (LDCC)



Item	*mm (Min/Max)*	*In (Min/Max)*	*Item*	*mm (Min/Max)*	*In (Min/Max)*
A	18.54/19.56	0.730/0.770	G	0.09/0.24	0.003/0.009
B	12.700/13.208	0.500/0.520	H	5.84/6.10	0.230/0.240
C*	15.24 TYP	0.600 TYP	I	31.75 TYP	1.25 TYP
D*	1.27 TYP	0.050 TYP	J	0.36/0.56	0.014/0.022
E	0.41/0.61	0.016/0.024	K*	1.75/1.90	0.069/0.075
F	2.03/2.79	0.080/0.110			

* At package body.

132 Pin Ceramic LDCC



Item	*mm (Min/Max)*	*In (Min/Max)*	*Item*	*mm (Min/Max)*	*In (Min/Max)*
A	23.75/24.51	0.935/0.965	F	0.09/0.24	0.004/0.008
B	18.67/19.43	0.750 TYP	G	5.08/7.62	0.200/0.250
C*	0.64 TYP	0.025 TYP	H	0.15/0.26	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	1.91 TYP	0.075 TYP
E	2.16/2.52	0.085/0.115	J*	20.32 TYP	0.800 TYP

* At package body.

Notes: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

132 Pin Ceramic LDCC Pin Identification

Pins	Function	Pins	Function
1, 2, 6-15, 17-27,	Input/Output	4, 16, 28, 42,	GND
31-33, 35, 36, 38-40,	Input/Output	57, 70, 82, 94,	GND
44-46, 48-51, 53-55,	Input/Output	108, 123	GND
59-61, 63, 64, 66-68,	Input/Output	3, 30, 41, 47, 52, 56,	Output GND
72-81, 84-93, 97-99,	Input/Output	69,96,107,113,118,122	Output GND
101,102, 104-106,	Input/Output	34, 37, 62, 65,	Output GND, or (+) Supply
110-112, 114-117,	Input/Output	100, 103, 128, 131	Output GND, or (+) Supply
119-121, 125-127, 129,	Input/Output	5, 29, 43, 58, 71,	(-) Supply
130, 132	Input/Output	83, 95, 109, 124	(-) Supply
		17	Most (-) Supply

Heat Sink and lid are electrically connected to the substrate which is in turn connected to pin 17.

V_{TT} = -2.0 Volts (Negative supply).

V_{CC} = Ø Volts (Clean ground), V_{CCA} = Ø Volts (Output ground).

V_{TTL} = +5.0 Volts. (Positive supply)

Connect both V_{CC} and V_{CCA} to a solid ground plane.

149 Pin Ceramic PGA Pin Identification

Pins	Function	Pins	Function
A2-A14, B1-B15, C1-C5,	Input/Output	H3, C7, N7,	GND
C11-C15, D1-D3, D13-D15,	Input/Output	C9, N9, H13	GND
E1-E3, E13-E15, F1, F2,	Input/Output	F3, G3, J3, K3,	Output GND
F14, F15, G1, G2, G14,	Input/Output	D5, M5, D11, M11,	Output GND
H1, H2, H14, H15, J1,	Input/Output	F13, G13, J13, K13	Output GND
J2, J14, J15, K1, K2,	Input/Output	E4, L4, L12, E12	Output GND, or (+) Supply
K14, K15, L1-L3, L13-L15,	Input/Output	C6, N6, C8,	(-) Supply
M1-M3, M13-M15, N1-N5,	Input/Output	N8, C10, N10	(-) Supply
N11-N15, P1-P15, R2-R14	Input/Output	D4	Most (-) Supply

Heat Sink and lid are electrically connected to the substrate which is in turn connected to pin D4.

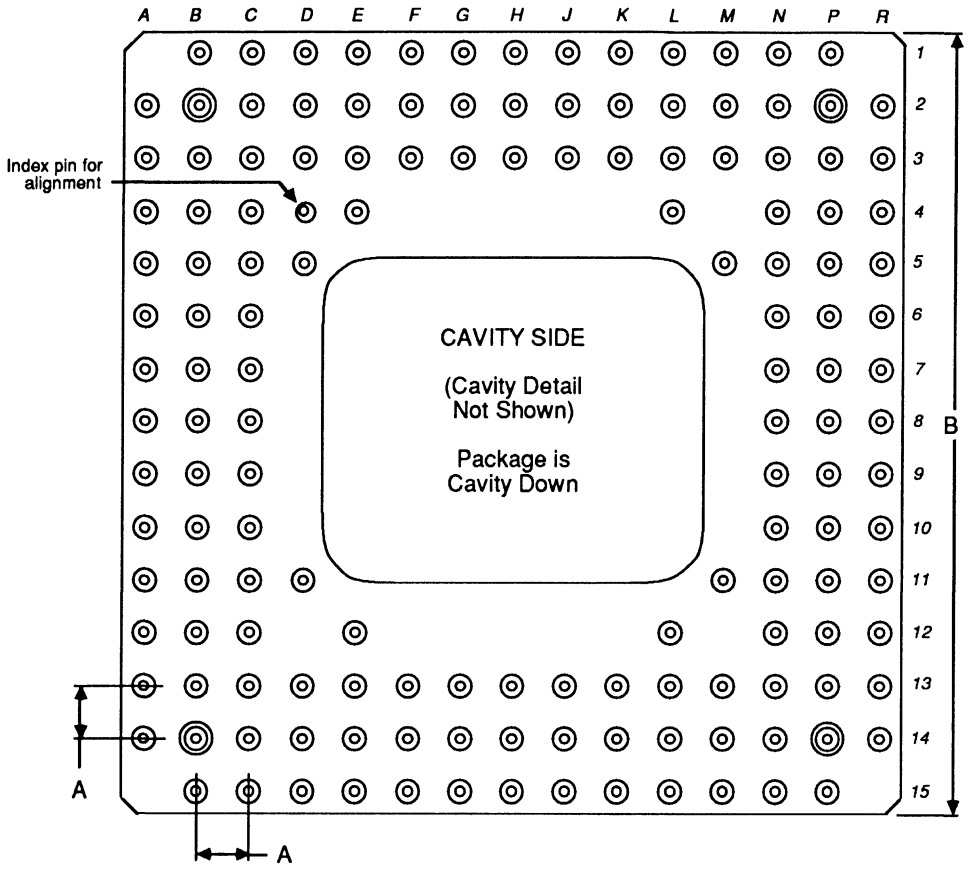
V_{TT} = -2.0 Volts (Negative supply).

V_{CC} = Ø Volts (Clean ground), V_{CCA} = Ø Volts (Output ground).

V_{TTL} = +5.0 Volts. (Positive supply)

Connect both V_{CC} and V_{CCA} to a solid ground plane.

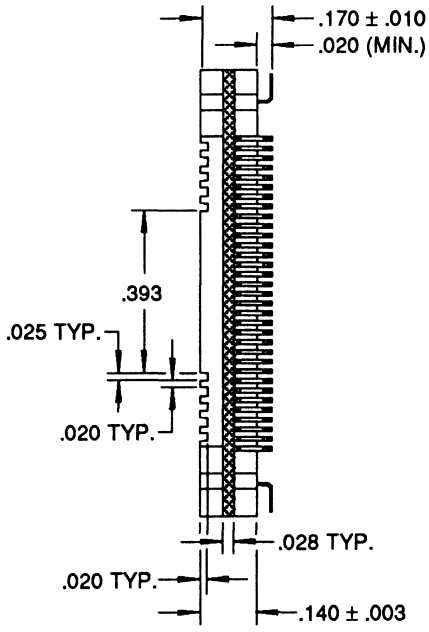
149 Pin Ceramic PGA



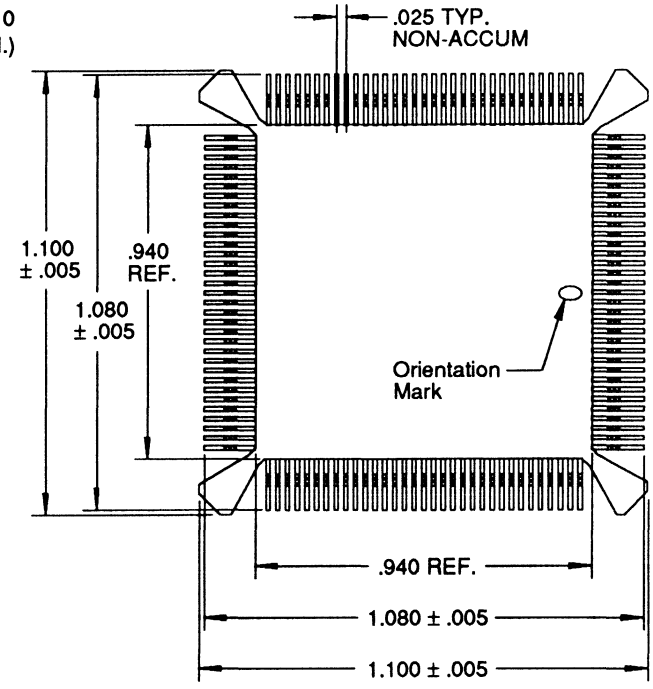
Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	2.54 TYP	0.100 TYP	E	2.25/2.92	0.085/0.115
B	37.85/38.61 SQ	1.490/1.520 SQ	F	27.40 TYP (Heatsink)	1.08 TYP (Heatsink)
C	0.41/0.51 DIA	0.016/0.020 DIA	G	0.38/0.63	0.015/0.025
D	4.45/4.95	0.175/0.195	H	1.14/1.40 (4 Plcs)	.050 TYP

Notes: 1) Drawing not to scale.
2) Package: Ceramic (alumina); Heat sink: Copper-tungsten; Leads: Alloy 42 with gold plating

132 Lead Metal Quad Flatpack Package Outline



SIDE VIEW



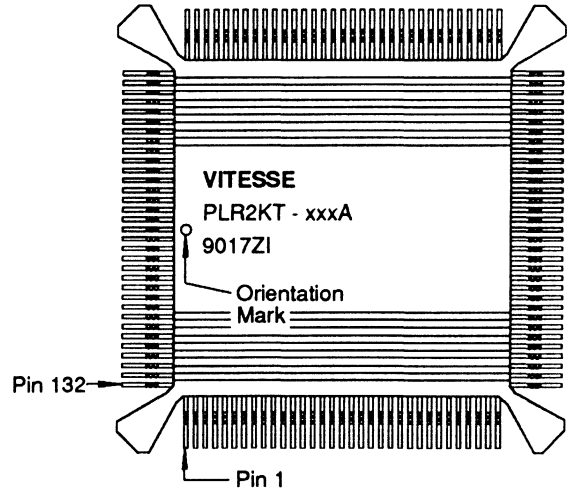
BOTTOM VIEW

Notes:

1) Drawing not to scale.

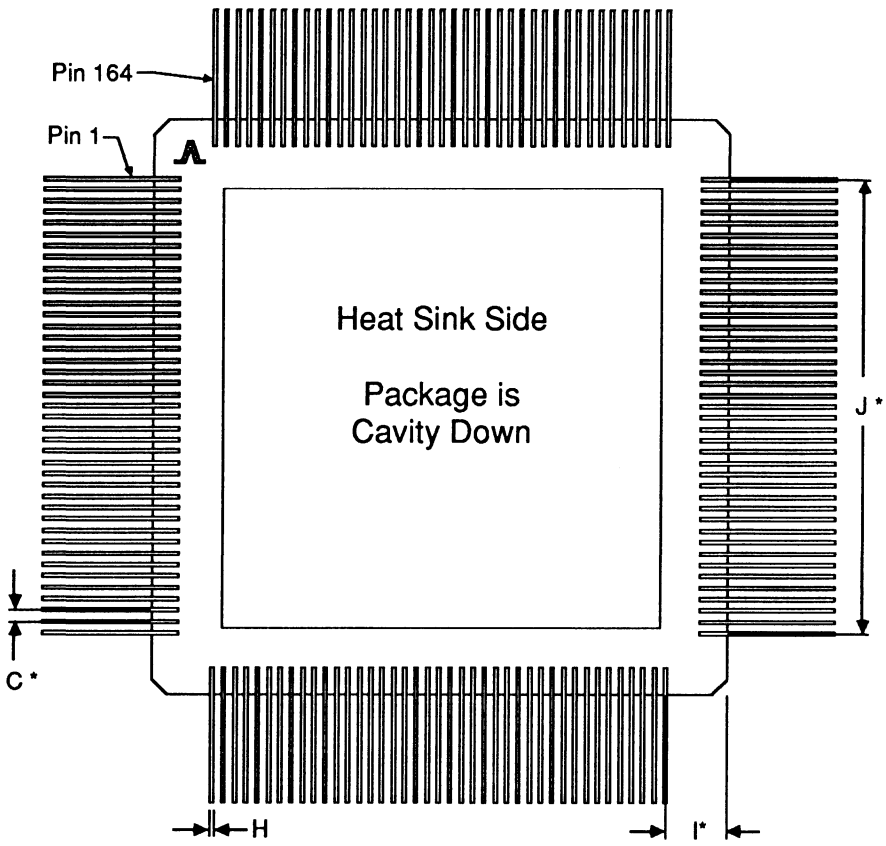
2) All non-toleranced dimensions are shown at nominal and tolerance is ± .010 unless otherwise noted.

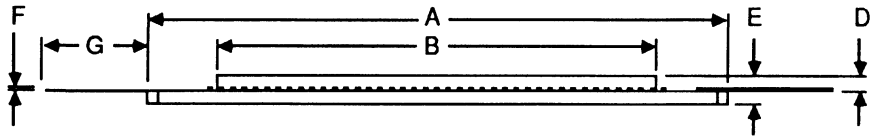
3) Package is black annodized Aluminum. Leads are copper alloy.



TOP VIEW

164 Pin Ceramic LDCC





Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	28.58/29.84 SQ	1.130/1.170	F	0.09/0.22	0.004/0.008
B	Ref 24 SQ	Ref 0.95 SQ	G	5.08/7.62	0.200/0.300
C*	0.64 TYP	0.025 TYP	H	0.15/0.25	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	Ref 1.91 TYP	Ref 0.075 TYP
E	2.16/2.92	0.085/0.115	J*	25.40 TYP	1.00 TYP

* At package body

Notes: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

164 Pin Ceramic LDCC Pin Identification

Pins	Function	Pins	Function
1,3,4,6,7,9,10,12,13,15,16,	Input/Output	8, 34, 47, 62, 77,	GND
18-20,22-24,26,27,29,30,32,	Input/Output	90, 116, 129, 159	GND
33,35,36,38,39,41,42,44,45,	Input/Output	11, 14, 17, 25, 28, 31,	Output GND
48-53,55-61,63-69,71-76,79,	Input/Output	43, 81, 93, 96, 99,	Output GND
80,82,83,85,86,88,89,91,92,	Input/Output	107, 110, 113, 125, 163	Output GND
94,95,97,98,100-102,	Input/Output	2, 5, 37, 40,	Output GND, or (+) Supply
104-109,111,112,114,115,	Input/Output	84, 87, 119, 122	Output GND, or (+) Supply
117,118,120,121,123,124,	Input/Output	21, 46, 54, 70, 78,	(-) Supply
126,127,130-135,137-143,	Input/Output	103, 128, 136, 152, 160	(-) Supply
145-151,153-158,161,162,164	Input/Output	144	Most (-) Supply

Heat Sink and lid are electrically connected to the substrate which is in turn connected to pin 144.

V_{TT} = -2.0 Volts (Negative supply).

V_{CC} = Ø Volts (Clean ground), V_{CCA} = Ø Volts (Output ground).

V_{TTL} = +5.0 Volts. (Positive supply)

Connect both V_{CC} and V_{CCA} to a solid ground plane.

211 Pin Ceramic PGA Pin Identification

Pins	Function	Pins	Function
A1-A17, B1-B17, C1-C17,	Input/Output	D4,D9,D14, E4,E14,J4,	GND
D1-D3, D6, D12, D14-D17,	Input/Output	J14,N4,N14,P4,P9,P14	GND
E1-E3, E13, E15-E17,	Input/Output	D5, D13, F4, F14,	Output GND
F1-F3, F15-F17, G1-G3,	Input/Output	M4, M14, P5, P13	Output GND
G15-G17, H1-H3, H15-H17,	Input/Output	E6, E12, H4, H14,	Output GND, or (+) Supply
J1-J3, J15-J17, K1-K3,	Input/Output	K4, K14, N6, N12	Output GND, or (+) Supply
K15-K17, L1-L3, L15-L17,	Input/Output	D7, D11, F5, F13,	(-) Supply
M1-M3, M15-M17, N1-N3,	Input/Output	M5, M13, P7, P11	(-) Supply
N5, N15-N17, P1-P3,	Input/Output	N13	Most (-) Supply
P6, P12, P15-P17, R1-R17,	Input/Output		
S1-S17, V1-V17	Input/Output		

Heat Sink and lid are electrically connected to the substrate which is in turn connected to pin N13.

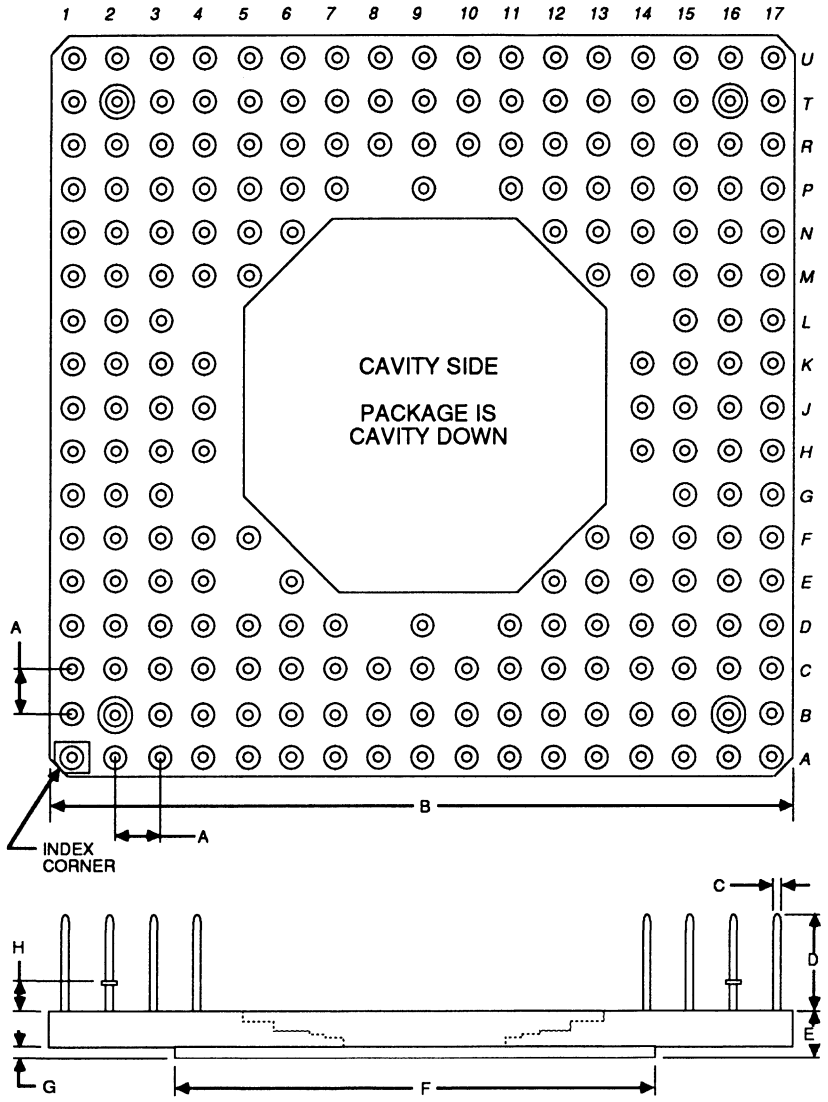
V_{TT} = -2.0 Volts (Negative supply).

V_{CC} = Ø Volts (Clean ground), V_{CCA} = Ø Volts (Output ground).

V_{TTL} = +5.0 Volts. (Positive supply)

Connect both V_{CC} and V_{CCA} to a solid ground plane.

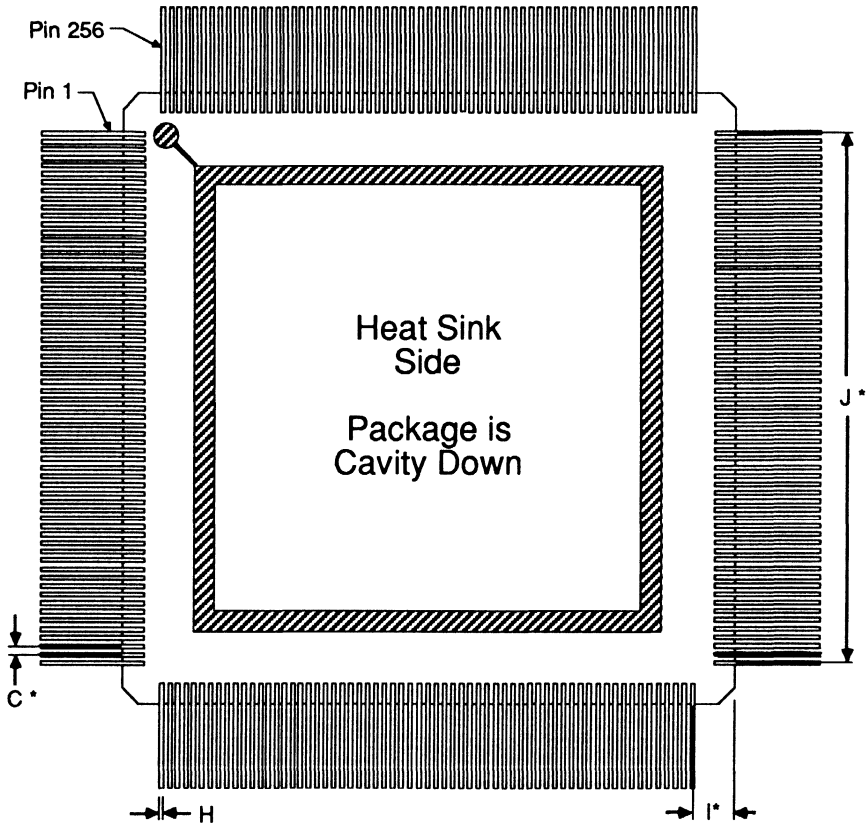
211 Pin Ceramic PGA



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	2.54 TYP	0.100 TYP	E	2.16/2.92	0.085/0.115
B	42.42/43.69	1.670/1.710	F	27.4 REF (Heatsink)	1.08 REF (Heatsink)
C	0.41/0.51 DIA	0.016/0.020 DIA	G	0.38/0.63	0.015/0.025
D	4.45/4.95	0.175/0.195	H	1.14/1.40 (4 Plcs)	.050 TYP

Notes: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

256 Pin Ceramic LDCC



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	36.57/37.59 SQ	1.440/1.480 SQ	F	0.09/0.216	0.004/0.008
B	TYP 28 SQ	TYP 1.00 SQ	G	5.08/7.62	0.200/0.300
C*	0.51 TYP	0.020 TYP	H	0.15/0.25	0.006/0.010
D	0.38/0.63	0.015/0.025	I*	REF 2.54 TYP	REF 0.100 TYP
E	2.16/2.92	0.085/0.115	J*	32.00 TYP	1.26 TYP

* At package body

Notes: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

256 Pin Ceramic LDCC Pin Identification

Pins	Function	Pins	Function
3-5,7-10,12-15,19-23,	Input/Output	2,17,33,49,64,70,88,106,	GND
25-28,30,31,34,35,37-40,	Input/Output	124,130,145,161,177,	GND
42-45,46,50-53,55-58,	Input/Output	192,198,216,234,252,253	GND
60-62,65-67,71-86,89-104,	Input/Output	6,11,54,59,134,	Output GND
107-122,126-128,131-133,	Input/Output	139,182,187	Output GND
135-138,140-143,147-151,	Input/Output	18,24,29,36,41,47,	Output GND, or (+) Supply
153-156,158,159,162,163,	Input/Output	68,125,146,152,157,	Output GND, or (+) Supply
165-168,170-174,178-181,	Input/Output	164,169,175,196	Output GND, or (+) Supply
183-186,188-190,193-195,	Input/Output	1,16,32,48,63,69,87,	(-) Supply
199-214,217-232,235-250,	Input/Output	123,129,144,160,176,	(-) Supply
254-256	Input/Output	191,197,215,233,251	(-) Supply
		105	Most (-) Supply

Heat Sink and lid are electrically connected to the substrate which is in turn connected to pin 105 in the 256 LDCC and pin 291 in the 344 LDCC.

V_{TT} = -2.0 Volts (Negative supply).

V_{CC} = Ø Volts (Clean ground), V_{CCA} = Ø Volts (Output ground).

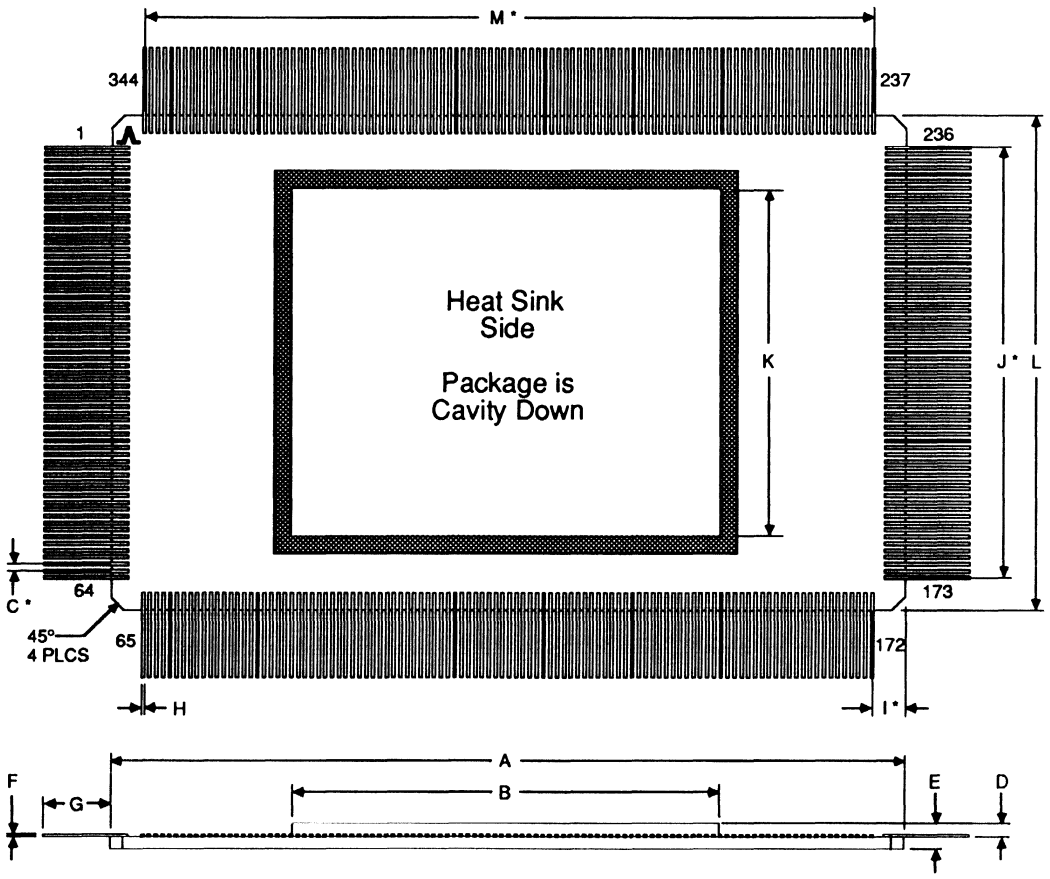
V_{TTL} = +5.0 Volts. (Positive supply)

Connect both V_{CC} and V_{CCA} to a solid ground plane.

344 Pin Ceramic LDCC Pin Identification

Pins	Function	Pins	Function
5-16,19-31,34-46,49-60,	Input	3,17,32,47,61,76,90,	GND
177-188,191-203,	Input	104,118,132,146,160,	GND
206-218,221-232	Input	175,189,204,219,233	GND
1, 64-68,70-73, 75,	Input/Output	248,262,276,290,304,	GND
78-80,82-85,87-89,92,	Input/Output	318,332	GND
94-97,99-102,106-109,	Input/Output	2,63,69,86,93,98,115,	Output GND
111-114,116-117,120,121,	Input/Output	122,139,144,151,168,	Output GND
123,124,125,126,128-131,	Input/Output	174,235,241,258,265,	Output GND
135-138,140-143,145,	Input/Output	270,287,294,311,316,	Output GND
148-150,152-155,157-159,	Input/Output	323,340	Output GND
162,164-167,169-173,	Input/Output	74,81,103,110,127,	Output GND, or (+) Supply
236-240,242-245,247,	Input/Output	134,156,163,246,253,	Output GND, or (+) Supply
250-252,254-257,	Input/Output	275,282,299,306,	Output GND, or (+) Supply
259-261,264,266-269,	Input/Output	328,335	Output GND, or (+) Supply
271-274,278-281,283-286	Input/Output	4, 18, 33, 48, 62, 77, 91,	(-) Supply
288,289,292,293,295-298,	Input/Output	105, 119, 133, 147, 161,	(-) Supply
300-303,307-310,312-315,	Input/Output	176, 190, 205, 220, 234,	(-) Supply
317,320-322,324-327,	Input/Output	249, 263, 277, 305, 319,	(-) Supply
329-331,334,336-339,	Input/Output	333	(-) Supply
341-344	Input/Output	291	Most (-) Supply

344 Pin Ceramic LDCC Pin Identification



Item	mm (Min/Max)	In (Min/Max)	Item	mm (Min/Max)	In (Min/Max)
A	58.93/59.94	2.320/2.340	H	0.15/0.25	0.006/0.010
B	35.54 TYP	TYP 1.36 SQ	I*	REF 2.54 TYP	REF 0.100 TYP
C*	0.51 TYP	0.020 TYP	J*	32.00 TYP	1.26 TYP
D	0.38/0.63	0.015/0.025	K	39.46 TYP	1.08 TYP
E	2.16/2.92	0.085/0.115	L	36.57/37.59 SQ	1.440/1.480
F	0.09/0.216	0.004/0.008	M*	54.36 TYP	2.140 TYP
G	5.08/7.62	0.200/0.300			

* At package body

Notes: 1) Drawing not to scale.
2) Packages: Ceramic (alumina); Heat sinks: Copper-tungsten; Leads: Alloy 42 with gold plating

Printed Circuit Board Considerations

Application Note 1

Introduction

Several important considerations must be taken into account when high speed GaAs (or ECL) ICs are interconnected on printed circuit boards. Chief among them is the need to properly terminate signal trace interconnections and the maintenance of low impedance ground and power supply connections.

This application note reviews some of the popular design techniques which are utilized to insure the integrity of high frequency signals on a printed circuit board. While these techniques have been used in ECL systems for some time, they may not be familiar to designers accustomed to CMOS circuits.

In general, signal traces on circuit boards should be treated as transmission lines if the propagation delay of the trace is more than one-tenth of the rise time of the signal. In the event that the propagation delay of the trace is short with respect to the rise time of the signal, any reflections caused by unterminated transmission lines are masked during the relatively slow transition and are not seen as overshoot or ringing.

Because most CMOS circuits have a high ratio of signal rise time to trace propagation delay, several inches of unterminated signal trace can be used without signal distortion. Since edge speeds in GaAs components are faster, the trace lengths must be considered as trans-mission lines and must be terminated properly to retain signal integrity.

Why are properly terminated transmission lines needed?

Rapidly changing signals require fast edge rates. A 200 MHz 50% duty cycle clock signal, for example, has a total period of 5ns. This period must accomodate a rise time, a fall time and some pulse width duration. As seen in figure 1, this signal can result in rise and fall times of approximately 1ns because of the desire to maintain the pulse signal integrity. Since GaAs circuits are designed to support signal rates beyond 200 MHz, both ECL compatible and 'native' GaAs compatible output drivers are designed for sub-nanosecond rise and fall times.

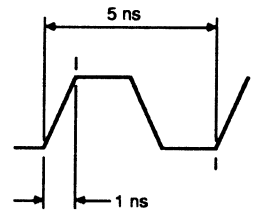


Figure 1: *200 MHz signal*

Such fast rise and fall time signals require that board signal traces are terminated trans-mission lines. Anytime that the propagation delay of a signal trace is longer than one-tenth the rise or fall time of the signal, an unterminated trace will result in voltage reflections which can cause degradations in the signal integrity.

Figure 2 shows the difference in signals observed in terminated and unterminated

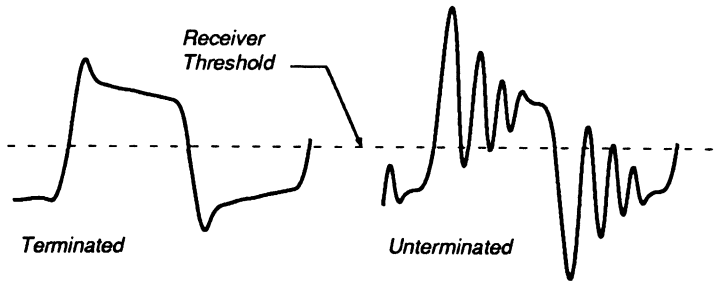


Figure 2: *Signals at terminated and unterminated signal traces*

environments. As seen, unterminated signal lines can result in substantial overshoot and ringing which are caused by voltage reflections.

These voltage reflections can cause a ringing signal which can be interpreted as several faster signals by the receiver. Terminated transmission lines eliminate voltage reflections and therefore produce clean waveforms. Generally, signals with sub-nanosecond rise and fall times must be terminated if the signal trace length is longer than 0.5 in. This is because the propagation velocity of a typical signal trace is approximately 2ns/ft.

Transmission Line Theory

Transmission line theory is important to an understanding of the methods used to terminate GaAs signal lines. Figure 3 shows a signal trace with typical loads at both ends. Usually, the signal trace delay is long when compared with the signal rise or fall time and reflections will appear at their full amplitude. The output voltage swing at point A, (V_A), is given by,

$$V_A = (V_{int})\left[\frac{Z_O}{R_O + Z_O}\right]$$

where V_{int} is the internal voltage swing, R_O is the chip output impedance and Z_O is the line impedance.

Since R_O is small compared to the line impedance, the output swing is nearly the same as the internal transition. The internal swing is approximately 1.4 V and the typical output swing is 1.3 V. The signal propagates down the line and is seen at point B some time, T_{pd}, later. The voltage reflection coefficient at the load end of the line, *rc*, is a function of the line characteristic impedance and the load impedance and is given by,

$$rc = \frac{(R_L - Z_O)}{(R_L + Z_O)}$$

where R_L is the termination load resistance and Z_O is the line impedance (both in ohms). If $R_L = Z_O$, there is no reflection. For any value of R_L close to Z_O, the reflection is small.

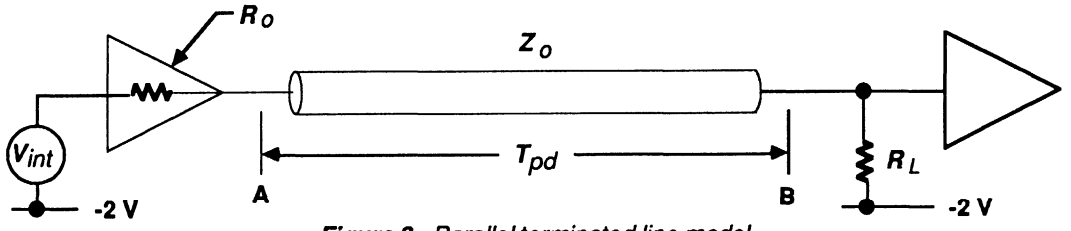


Figure 3: Parallel terminated line model

Practical Transmission Lines

The key to maintaining signal integrity in practical high frequency digital systems is the utilization of properly terminated, controlled impedance transmission lines. Controlled impedance transmission lines can be realized in several ways. For signal transmission over long distances, coaxial cables or twisted pairs are popular. Some common types of coaxial cable have characteristic impedances of 50, 75, 93 or 125 ohms. Twisted pairs can be made from AWG 24-28 hook-up wire twisted about 30 turns per foot. Such twisted pairs have a characteristic impedance of about 110 ohms.

For signal transmission within a circuit board, Striplines and Microstrip lines are usually used. A Microstrip line is shown in figure 4. It is constructed with a strip conductor for the signal line separated from a ground plane by a dielectric. The signal line is made by etching away the unwanted copper using photoresist techniques. If the thickness, width of the line, and the distance from the ground plane are controlled, the line will exhibit a predictable characteristic impedance that can

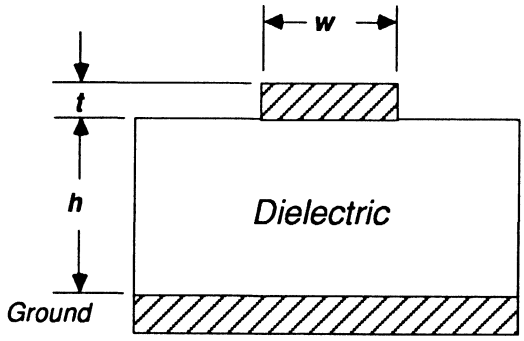


Figure 4: Microstrip

be controlled to within 5%. The characteristic impedance, Z_O, of a Microstrip Line can be approximated by:

$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left[\frac{5.98h}{0.8w + t}\right]$$

where e_r is the relative dielectric constant of the board material (which is typically 5 for FR-4 fiber-glass epoxy boards), and w, h and t are the dimensions indicated in figure 4 in inches.

The propagation delay of the line may be approximated by:

$$T_{pd} = 1.017\sqrt{0.475\, e_r + 0.67}\ ns/ft$$

Note that the propagation delay of the line is dependent only on the dielectric constant and is not a function of line width or spacing. For FR-4 fiber-glass epoxy boards, the propagation delay of the Microstrip line is approximately 1.8 ns/ft.

A Stripline is shown in figure 5. It consists of a copper ribbon centered in a dielectric medium between two conducting planes. If the thickness and width of the line, the dielectric constant medium, and the distance between the ground planes are all controlled, the line will exhibit a characteristic impedance that can be held constant within 5%. The characteristic impedance of a Strip Line is given by,

$$Z_O = \frac{60}{\sqrt{e_r}} \ln\left[\frac{4b}{0.67\pi w\,(0.8 + t/w)}\right]$$

where e_r is the relative dielectric constant of the medium and b, t, and w are the dimensions shown in figure 3. This equation proves accurate for,

$$\frac{w}{(b - t)} < 0.35 \text{ and } \frac{t}{b} < 0.25$$

and the propagation delay of the line is,

$$t_{pd} = 1.017\sqrt{e_r}\ ns/ft$$

For FR-4 fiber-glass epoxy, the propagation delay of the Stripline is about 2.27 ns/ft. Note that in both Striplines and Microstrip, the propagation delay is not a function of the width or spacing.

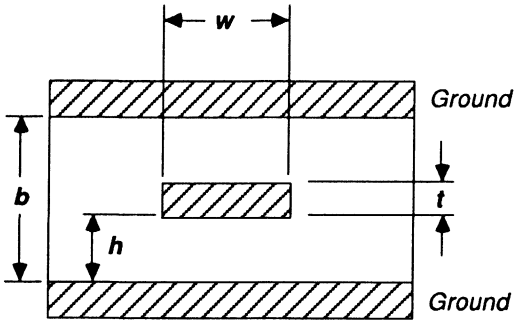


Figure 5: Stripline

Parallel Terminated Lines

Parallel terminated lines such as the one shown in figure 3 are used for fastest circuit performance. Standard output drivers on Vitesse's GaAs products can drive 50 ohm lines. ASIC products also allow for up to 25 ohm drive capability. In each case the term "line" refers to a signal transmission line, terminated at the receiving end through a resistor of the characteristic line impedance to -2 Volts. With parallel terminated lines, the line termination supplies the output pull-down current for the open source-follower output FET. Thus, no other pull-down resistor is required at the output of the driving gate.

Power Distribution

Power distribution is an important factor in system design. The loss of noise margin due to reduced power supply voltage or noise on the power supply lines means a reduction in the circuit tolerance to crosstalk and ringing. Points to consider for overall system operation include total circuit and termination power, voltage drops on the power busses, and noise induced on the power distribution lines by the circuits and by external sources.

Vitesse GaAs circuits are designed to interface with each other over a power supply voltage range of ± 5% from the nominal -2 Volts without a loss of noise margin. However, if two chips are at different supply voltages or on the same power supply with a voltage offset between them, there will be a predictable loss of noise margin.

The main causes of V_{TT} power supply offsets between circuits are:

- Inadequate power busses to handle the necessary current
- Separate supplies with common positive terminals at slightly different potentials
- Separate positive grounded supplies with an inadequate number of interconnection ground bus bars

Power supply requirements for Vitesse GaAs circuits must take into account the fact that a 50 ohm ECL compatible output sources about 22 mA in a logic HIGH state and no current in a logic LOW state. The 22 mA differential between the two states can produce a significant power supply current fluctuation. Such an effect should be considered when specifying the power supply.

Current fluctuations are by no means insurmountable. Brief current changes are smoothed by bypass capacitors at the power supplies. Also, the typical 50% distribution of output logic levels (e.g., HIGH and LOW states) tends to minimize current changes.

High frequency noise and ripple from the power supply should be avoided. These effects produce differences in voltage levels among sections of a system and lead to loss of noise margin. As a rule of thumb, noise can be considered "high frequency" whenever the mean wave length of the noise (in units of time) is not more than 2 times greater than the propagation delay of the longest power line. For implementations which use GaAs ICs, it is recommended that high frequency power supply noise be held to under 25 mV of total signal variation.

When multiple power supplies are used, the positive terminals should be connected together with a large bus and the output voltages maintained as equal as possible. It is desirable to keep the power supply levels within 25 mV of one another.

To achieve the requirements imposed by GaAs circuits on power supply distribution, printed circuit boards with large ground and power planes are commonly used. Power supply bypass capacitors are used on the circuit boards to handle the current transients required by the outputs.

Typically, a 1 to 10 microfarad capacitor is placed on the board at the power supply inputs and a 0.1 to 0.01 microfarad capacitor is connected between ground and -2 V on every V_{TT} package pin. RF type capacitors are recommended because of their low inductance.

Interfacing GaAs Products to ECL/TTL

Application Note 2

Introduction

Vitesse GaAs products are designed to interface to external circuits with standard ECL and TTL signal levels. In some cases, however, slight differences exist between the signal levels produced by these compatible parts and actual silicon ECL or TTL components.

Although Vitesse components use GaAs DCFL circuitry internally, the I/O is designed to interface directly with industry standard ECL and TTL levels. In addition, the FURY Series of gate arrays, the VCB50K Standard Cells and the VS12G476 4K SRAM can send and receive signals at Vitesse's own internal GaAs levels, thus allowing one device to "talk" directly to another device with no translation delays. Figure 1 shows the model used to specify system noise margins.

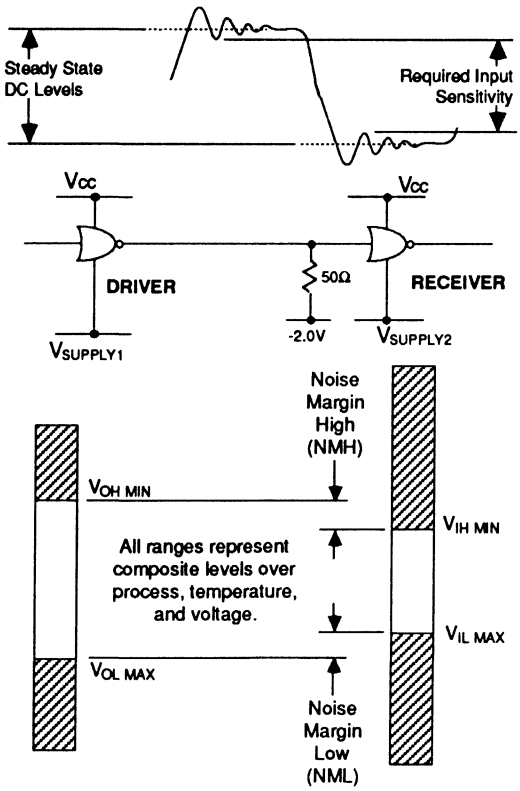


Figure 1: *Noise Margin Model*

ECL I/O

Industry standard ECL I/O signal levels are based on voltage levels that result naturally from the characteristics of bipolar logic families. In order to interface with standard ECL logic, Vitesse components use buffered level translators at the input and output pads. The input translator consists of a differential current switch which drives a level shifter. The reference voltage for the differential pair can be provided in one of three ways:

1. Internal Reference

This option uses the internal reference on the chip. No additional pins are required. Noise margins for this scheme are shown in table 1.

2. External Band-Gap Diode

This option is shown in figure 2 and involves the use of an LM185 diode in conjunction with a gate array or standard cell product. The user must connect the LM185 to the external reference pin on the GaAs device. Use of the external diode reference provides improved input noise margins (see table 2) over a wider V_{TT} range of -2.0V ± 10%.

3. Full External Reference

The user may provide an external reference voltage of -1.32V ± 25 mV to the external reference pin. (See table 3 for noise margins.) AN-8 discusses the creation of an external

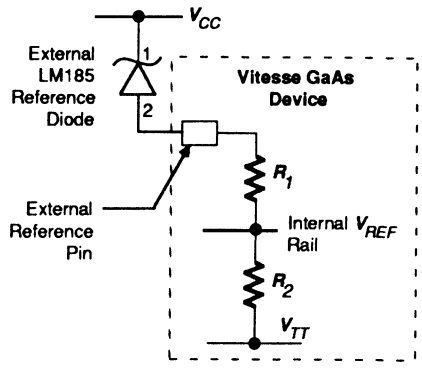


Figure 2: *External Band-Gap Diode Reference*

Table 1: ECL Noise Margins Using the Internal Reference

Noise Margin	ECL Device Driving Vitesse Device		Vitesse Device Driving ECL Device	
	ECL 100K	ECL10KH	ECL 100K	ECL10KH
HIGH	75 mV	80 mV	145 mV	150 mV
LOW	80 mV	60 mV	145 mV	140 mV

Table 2: ECL Noise Margins Using an External Diode Reference

Noise Margin	ECL Device Driving Vitesse Device		Vitesse Device Driving ECL Device	
	ECL 100K	ECL10KH	ECL 100K	ECL10KH
HIGH	100 mV	105 mV	145 mV	150 mV
LOW	110 mV	90 mV	145 mV	140 mV

Table 3: ECL Noise Margins Using a Full External Reference

Noise Margin	ECL Device Driving Vitesse Device		Vitesse Device Driving ECL Device	
	ECL 100K	ECL10KH	ECL 100K	ECL10KH
HIGH	140 mV	145 mV	145 mV	150 mV
LOW	145 mV	125 mV	145 mV	140 mV

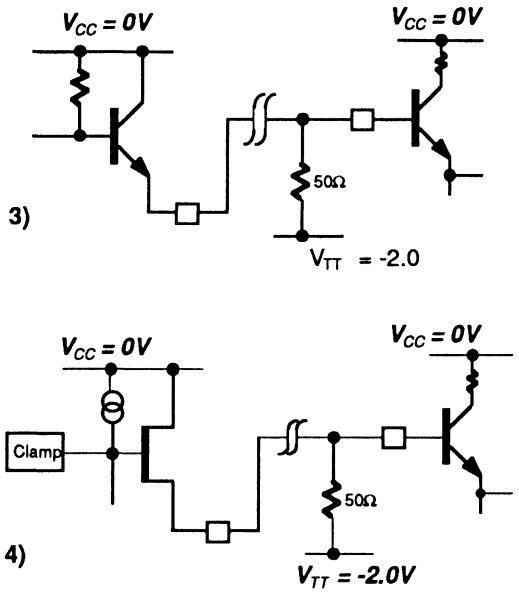
Notes:
1) Worst case noise margins over nominal conditions.
2) Source for ECL 100K DC characteristics: Fairchild F100K DC Family Specifications.
3) Source for ECL 10KH DC characteristics: Motorola MECL 10KH DC Family Specifications.

reference using the LM185.

Different but equally important issues arise when interfacing Vitesse components' output (or any "non-bipolar" ECL output) with a silicon bi-polar ECL circuit input. Figures 3 & 4 illustrate this situation. In figure 3, an ECL input is the base of an NPN bipolar transistor whose collec-tor is connected to V_{CC} (0 Volts). In order not to degrade the switching characteristics of this input, it is essential that this input transistor be kept out of saturation, which means that the base collector diode must not become forward biased. This condition is assured when driving this input with a bipolar ECL output, since the emitter follower output cannot go more positive than one diode drop below V_{CC}.

The situation is different when the output emitter follower is replaced with a FET such as in figure 4. Vitesse's ECL output driver incorporates clamp circuitry to ensure that the output high level does not go more positive than -700mV.

One major difference between Vitesse ECL compatible outputs and silicon ECL outputs is that Vitesse outputs are "cutoff" drivers which have an output low voltage equal to the V_{TT} supply. In this way, a logic low is also a high impedance state and several outputs can be bussed together.



Figures 3 & 4: *Bipolar & GaAs ECL outputs driving an ECL input*

TTL I/O

Vitesse ASICs support TTL inputs and outputs in addition to ECL and GaAs I/O. The standard minimum input swing specification at a TTL input is ≥1.2 V (0.8 - 2.0 V) compared to 310 mV for ECL. Figure 5 shows the guaranteed worst case TTL I/O levels in Vitesse components. The TTL inputs source a worst case current of -500 µA.

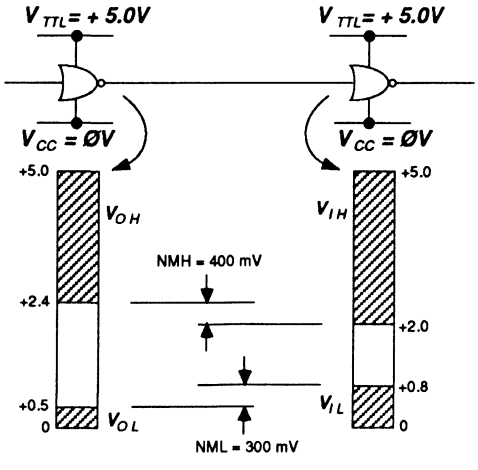
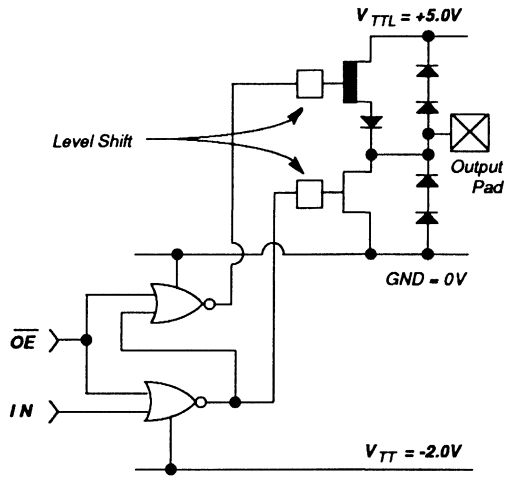


Figure 5: *Worst Case TTL I/O Levels for Vitesse Products*



Figures 6: *TTL Output Buffer Schematic*

TTL compatible outputs impose certain constraints on the user. Figure 6 is a schematic representation of the TTL output buffer with tri-state capability.

One difference between the Vitesse TTL totem-pole output and typical silicon TTL is that the high level (V_{OH}) typically goes higher in the Vitesse output. The high level can be one diode drop below V_{TTL} (+5.0 V), whereas in standard TTL, the output generally does not exceed 3.8 Volts. The low level (V_{OL}) is similar to standard TTL (≥ 0.4 Volts) with the rated sinking current (8 mA).

The TTL output tri-state current voltage characteristics are also different from typical silicon bipolar devices. Figure 7 shows the TTL output tri-state I-V curve. Note that the tri-state leakage current, I_{OZ}, shows a sharp increase near 3.5 Volts. This voltage is low, but well beyond the TTL valid high level of 2.4 Volts. In a typical system application, there may be many TTL outputs from the Vitesse component bussed together with either CMOS or TTL open collector outputs. The output high level on the bus equilibriates at an operating point (Q point) consistent with the I-V characteristics shown in figure 7 and the current sourcing capability of the driving device.

The output edge rates in the Vitesse TTL outputs are intrinsically fast (see figure 8). With 30 pF capacitive load, the edge rates are about

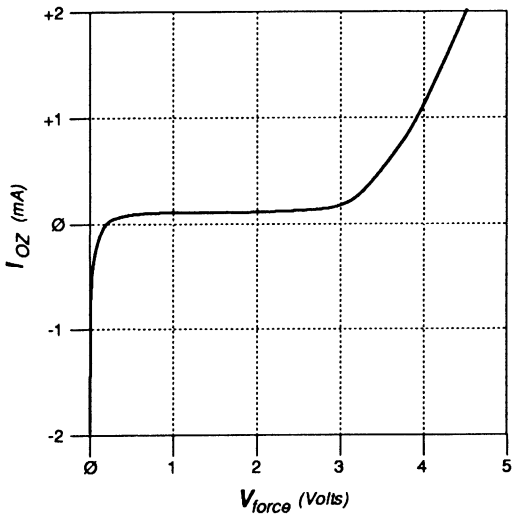


Figure 7: *TTL Output Tri-State I-V Curve*

3 ns. Handling very fast edge rates on TTL circuit boards is difficult due to the severe ringing that fast edges produce. To control the ringing on the circuit board, it is helpful to buffer the TTL outputs with a silicon bus interface chip such as the 74244.

GaAs I/O Levels

The FURY Series Gate Arrays, the VCB50K Standard Cells and the VS12G476 4K SRAM support inputs and outputs which switch at internal DCFL GaAs levels. Figure 9 shows the noise margins when using a GaAs level output to drive a GaAs input. The designer should note that the GaAs I/O levels will track directly with changes in V_{TT}.

The GaAs I/O buffers allow the designer to interface GaAs devices directly without having to undergo the delay and power required for the logic level translations.

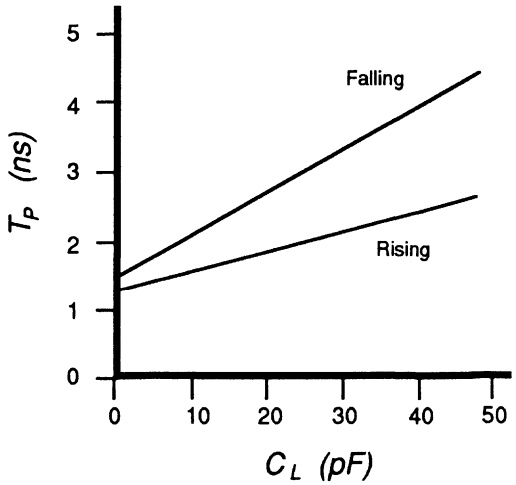


Figure 8: *Capacitive Loading Effect on Vitesse TTL Output Buffers*

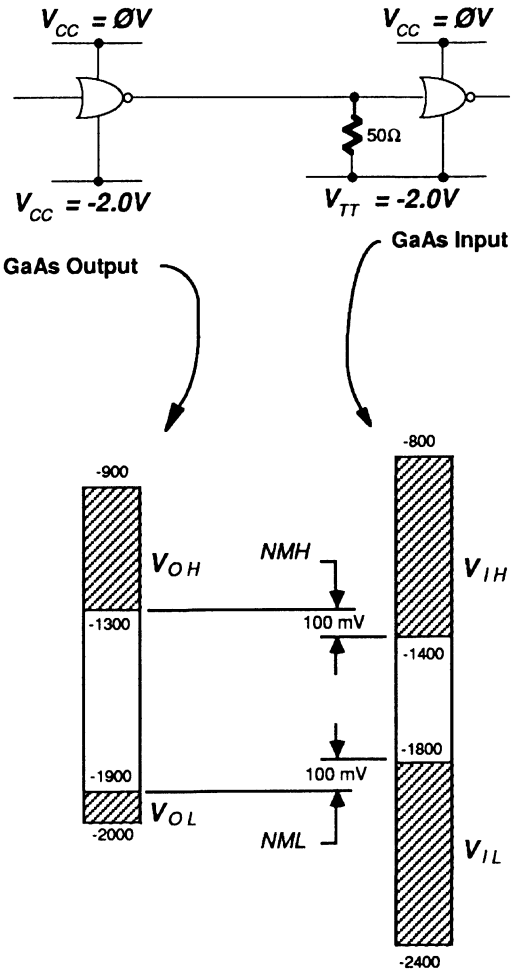


Figure 9: *GaAs Ouput Driving a GaAs Input*

DC Specifications

The following tables (4-9) taken from the FURY Series Gate Array Design Manual are representative of all of Vitesse's GaAs devices. Tables 4, 5 and 6 give DC specifications for the ECL I/O cells using the internal reference, an external diode reference, or a full external reference, respectively. DC specifications for TTL I/Os are in Table 7, and Table 8 gives the DC specifications for GaAs I/Os. The designer should note that the GaAs I/O levels track with changes in V_{TT}. Following the tables are specified Recommended Operating Conditions and Absolute Maximum Ratings.

Table 4: *DC Characteristics for ECL I/O Cells Using Internal Reference*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1020	-850	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1100	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1540	mV	Guaranteed LOW for all inputs

Notes: Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load = 50Ω to V_{TT}.

Table 5: *DC Characteristics for ECL I/O Cells Using External Diode Reference*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1025	-850	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1125	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1510	mV	Guaranteed LOW for all inputs

Notes: Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load = 50Ω to V_{TT}.

Table 6: *DC Characteristics for ECL I/O Cells Using Full External Reference*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	-1025	-850	-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	-2000	—	-1620	mV	
V_{IH}	Input HIGH voltage	-1165	—	-700	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	-2000	—	-1475	mV	Guaranteed LOW for all inputs

Notes: Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load = 50Ω to V_{TT}.
External reference = -1.32V ± 0.025V.

Recommended Operating Conditions

ECL Supply Voltage *(V_{CC}), (V_{TT})* ..... -2.0V ± 5%

TTL Supply Voltage, *(V_{TTL})* ..... +5.0V to +5%

Operating Temperature [2], *(T)* .....(Commercial) 0° to 70°C, (Industrial) -40° to +85°C, (Military) -55° to +125° C

NOTE: 1) When using internal ECL 100K reference level.

2) Lower limit of specification is ambient temperature and upper limit is case temperature.

Table 7: *DC Characteristics for TTL I/O Cells (Over recommended operating conditions, TTLGND = GND)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	V_{TTL}	V	I_{OH} = -2.4 mA
V_{OL}	Output LOW voltage	0	—	0.5	V	I_{OL} = 8 mA
V_{IH}	Input HIGH voltage	2.0	—	V_{TTL}	V	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	0	—	0.8	V	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	50	µA	$V_{IN} = V_{TTL}$
I_{IL}	Input LOW current	-500	—	—	µA	V_{IN} = 0.5 V
I_{OZH}	3-state output OFF current HIGH	—	—	100	µA	V_{OUT} = 2.4 V
I_{OZL}	3-state output OFF current LOW	-100	—	—	µA	V_{OUT} = 0.5 V
I_{OH}	Open collector output leakage current	—	—	100	µA	V_{OUT} = 2.4 V

Table 8: *DC Characteristics for GaAs I/O Cells (Over recommended operating conditions, $V_{CC} = V_{CCA}$ = GND, Output load = 50Ω to V_{TT}.)*

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	V_{TT}+700	—	V_{TT}+1100	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}	—	V_{TT}+100	mV	
V_{IH}	Input HIGH voltage	V_{TT}+600	—	V_{TT}+1200	mV	Guaranteed HIGH for all inputs
V_{IL}	Input LOW voltage	V_{TT}-400	—	V_{TT}+200	mV	Guaranteed LOW for all inputs
I_{IH}	Input HIGH current	—	—	200	µA	$V_{IN} = V_{IH}$ max
I_{IL}	Input LOW current	-100	—	—	µA	$V_{IN} = V_{IL}$ min

Note: 1) Differential GaAs output pins must be terminated identically.
2) If only GaAs I/Os are used, V_{TT} = 0V, V_{CC} = +2.0V, and all I/O levels are still referenced to V_{TT}.

Absolute Maximum Ratings (1)

Potential Pin to Ground, (V_{TT}) ..... -2.5V to +0.5V
Potential Pin to Ground, (V_{TTL}) ..... +6.0V to -0.5V
ECL Input Voltage Applied (2), ($V_{IN\ ECL}$) ..... +0.5V to V_{TT}
TTL Input Voltage Applied (2), ($V_{IN\ TTL}$) ..... -0.5V to V_{TTL}
ECL or TTL Output Current, I_{OUT}, (DC, output HIGH) ..... 50 mA
Maximum Junction Temperature, (T_j) ..... 150°C
Case Temperature Under Bias, (T_C) ..... -55° to +125°C
Storage Temperature (T_{STG}) ..... -65° to +150°C

NOTES: 1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

2) V_{TT}, V_{TTL} must be applied before any input signal voltage and V_{ECLIN} input must be greater than V_{TT} - 0.5V.

3) Lower limit of specification is ambient temperature and upper limit is case temperature.

Packaging

Application Note 3

Introduction

The reliable operation of high performance GaAs ICs is largely dependent on the design of the package. High speed digital signals must be efficiently transferred from the IC to the PC board and vice-versa. Because the performance of a semiconductor device is effected by increasing temperature, the thermal properties of the packaged component are also important. This application note describes the electrical characteristics and thermal considerations for Vitesse standard packages.

Vitesse supports a full range of ceramic packages for its products. These include dual in-line packages (DIPs), leaded and leadless chip carriers (LDCC, LCC), and pin grid arrays (PGAs). All packages are multilayer construction with controlled (50 Ω) impedance signal traces and power and ground planes for use in high speed digital applications. These packages are designed with the cavity down and incorporate a copper-tungsten heat spreader for heat sink attachment.

Package Electrical Characteristics

Figure 1 illustrates the configuration of a typical FURY ECL-compatible output and its electrical model. Today's high speed circuit design demands that an IC package deliver the edge rates generated by the transistor to the circuit board trace. The transmission of fast edge rates is complicated by the parasitic in-ductance and capacitance associated with the package

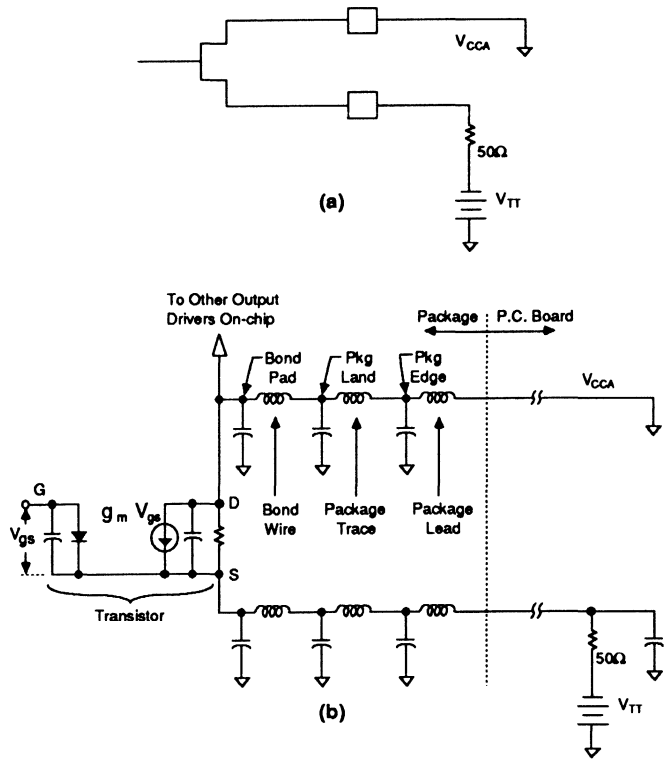


Figure 1: ***a)*** *On-Chip Output Driver* ***b)*** *Package Electrical Model*

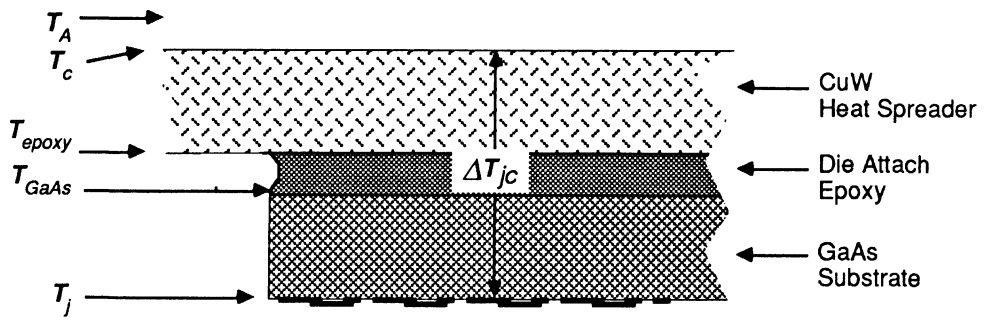
traces and bond wires. These demands are particularly stringent on the power supply lead which must generally supply current to several transistors. The voltage drops generated by circuit outputs switching $[\Delta V = L(\Delta I/\Delta t)]$ can cause "glitches" on the chip power busses. In the design of Vitesse chips and packaging, these problems are minimized in the following ways:

- ECL outputs either have their own dedicated VCCA pin or share a VCCA pin with at most three other transistors
- The larger packages contain high-frequency bypass capacitors inside the die cavity.
- Power supply planes rather than traces are utilized in the package to minimize power supply lead inductance
- VCC (for logic) and VCCA (for outputs) have separate pads on-chip and are connected to separate package pins.
- The package die cavity closely matches the die size to minimize bond wire length.
- Multiple power supply pads on-chip.
- Each FURY die has a separate metal layer for power and ground distribution on-chip. This not only improves internal noise margins but also minimizes on-chip inductance.

Because Vitesse has taken these precautions in its products, standard ECL design techniques can be used for the construction of printed circuit boards. Special modifications to accomodate Vitesse's products are, in general, not necessary.

Package Thermal Considerations

When implementing any ASIC-based design, one must be aware of the thermal environment of the chip in order to ensure that the heat produced by the IC can be effectively dissipated so the maximum rated junction temperature is not exceeded. This reduces the risk of failure by mechanisms such as electromigration.



Legend:

T_j = junction temperature
T_{GaAs} = temperature at backside of die
T_{epoxy} = temperature at inside surface of heat spreader
T_c = outside case temperature
T_A = ambient temperature
ΔT_{jc} = difference between the junction and outside case temperature

Figure 2: *Enlarged cross section of GaAs die attached to package heat spreader*

Thermal Calculation Example - VSC15K

Figure 2 shows the heat flow path from the device junction to the ambient. A sample calculation illustrates the heat flow problem quantitatively for a VSC15K design in a 211 PGA package.

Given that:

Chip area = 8128 µm x 7112 µm
= 5780 µm² or 0.578 cm²
Power diss. = ***P***

Referring to figure 2 and using the thermal conductivities,

K_{GaAs} = 0.55 W/°C•cm,
K_{epoxy} = 0.0186 W/°C•cm,
K_{CuW} = 1.63 W/°C•cm

we can then calculate the thermal impedance from junction to case.

$$\theta_{GaAs}=\left(\frac{1}{K_{GaAs}}\right)x\frac{0.066\ cm}{0.578\ cm^2}=0.21°\ C/W$$

$$\theta_{Epoxy}=\left(\frac{1}{K_{Epoxy}}\right)x\frac{0.0056\ cm}{0.578\ cm^2}=0.47°\ C/W$$

$$\theta_{CuW}=\left(\frac{1}{K_{CuW}}\right)x\frac{0.05\ cm}{0.578\ cm^2}=0.05°\ C/W$$

Total impedance from junction to case is:

θ_{jc} = 0.73 °C/Watt

and the overall temperature rise from junction to case is:

$\Delta T_{jc} = \theta_{jc} \times P$ + Local micro-rise

The micro-rise is a factor which is due to the local heating that occurs at the device junction, and can be estimated to be about 5 °C. Thus, for an implementation which dissipates 7 Watts,

ΔT_{jc} = (0.73 °C/W x 7.0W)+5 °C = 10.1 °C.

In the FURY Series commercial grade parts, the recommended maximum operating junction temperature is limited to 90 °C. Given an ambient temperature of 60 °C, the maximum difference in temperature from junction to ambient which can be allowed is 30 °C. With power dissipation at about 7 Watts for the part, a heatsink combined with airflow must be used to yield a total junction-to-ambient thermal resistance (θ_{ja}) of 4.3 °C/W or less. From our previous calculation we found that for a 7W part, the junction-to-case temperature rise will be approximately 10.1 °C . Thus, the case-to-ambient temperature rise ($\Delta T_{jA} - \Delta T_{jc}$) must be less than 19.9 °C, and therefore the case-to-ambient thermal resistance must be 2.84 °C/W or less (19.9 °C/7W = 2.84 °C/W). This will require only a moderately efficient heatsink with a surface area on the order of 20 in².

Several manufacturers supply heat sinks suitable for Vitesse ASICs. Two leading manufacturers are:

EG&G Wakefield Engineering
60 Audubon Rd.
Wakefield, MA 01880

Thermalloy, Inc.
2021 W. Valley View Ln.
Dallas, TX 75381-0839

When a heat sink is selected for a Vitesse ASIC, it is important to obtain an accurate θ_{ca} curve for the heat sink from the manufacturer. By using this information and the 'θ' for the epoxy used to attach the heat sink to the package, curves showing the relationship of junction temperature to air flow can be generated.

Additional information relating to specific packages for Vitesse ASICs can be obtained from the Design Manual for that product. Also, "air curves", which show the thermal performance of Vitesse packages as a function of air flow, can be obtained from a Vitesse Applications Engineer.

7

Generation of a -2 Volt Supply from a +5 Volt Supply

Application Note 4

Description

Some Vitesse ASIC products need both -2V and +5V power supplies. This application note describes a method of generating a -2V supply from a +5V supply. It is possible to generate the -2V supply from a standard +5V supply, commonly found in TTL systems, by using a switching regulator IC such as the LT1070 from Linear Technology Corp. (Milpitas, CA).

The LT1070 is a monolithic high power switching regulator which can be configured with the aid of a few external components to create a positive input - negative output Flyback Converter. The schematic below depicts a Flyback Converter configuration capable of +5V to -2V conversion. In addition to the LT1070, the circuit includes a standard LM124 op-amp from National Semiconductor Corp. (Santa Clara, CA) and a PE-65108 Transformer from Pulse Engineering (San Diego, CA). Such a circuit is capable of delivering up to 4 Amps of continuous current at -2 Volts and has line regulation of 0.05%/V.

Additional information on the LT1070 and the Output Flyback Converter configuration can be obtained from Linear Technology Corp.

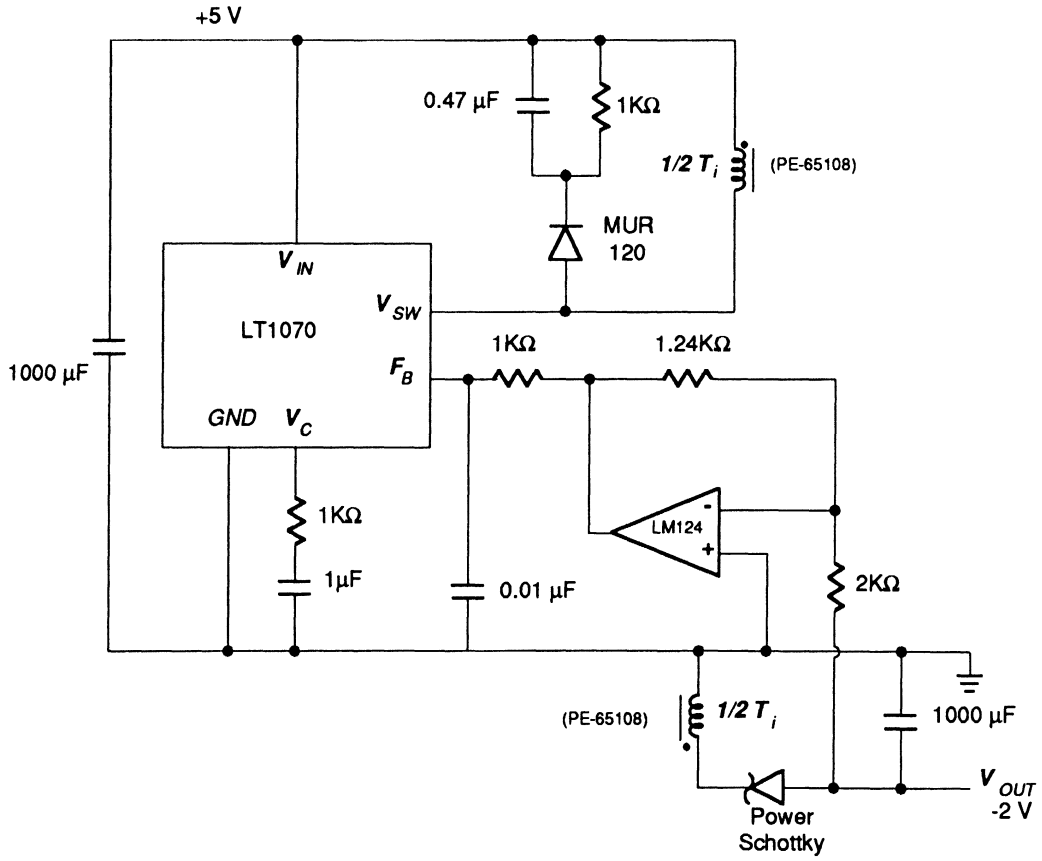


Figure 1: *Flyback Converter Configuration*

SONET and the VS8010 Series

Application Note 5

Introduction

This application note describes the SONET (Synchronous Optical NETwork) transmission standard and how the VS8010 Series of ICs can be used to implement SONET. Background information is included on both SONET and the VS8010 Series. A detailed description of SONET conventions and their interface with the features of the VS8010 product family is included as well. A list of specific optical transmitters and receivers which are compatible with the VS8010 Series multiplexers and demultiplexers is also provided.

The VS8010 Series

The VS8010 series of integrated circuits are a set of high speed GaAs multiplexers and demultiplexers intended for applications in optical fiber telecommunication links which are intended to comply with the Synchronous Optical NETwork (SONET) transmission standard. The series is comprised of three chips. They are: the VS8011 multiplexer, VS8012 demultiplexer and frame recovery circuit, and the VS8010 which combines the multiplexer, demultiplexer and frame recovery circuits into one monolithic entity.

These chips are the result of a collaborative research agreement between Vitesse Semiconductor Corporation and Bell Communications Research (Bellcore). Each chip represents a different personalization of the Vitesse VSC1500 gate array. The VSC1500 is an ASIC device which is optimized for multiplexer or demultiplexer applications. Figure 1 depicts the

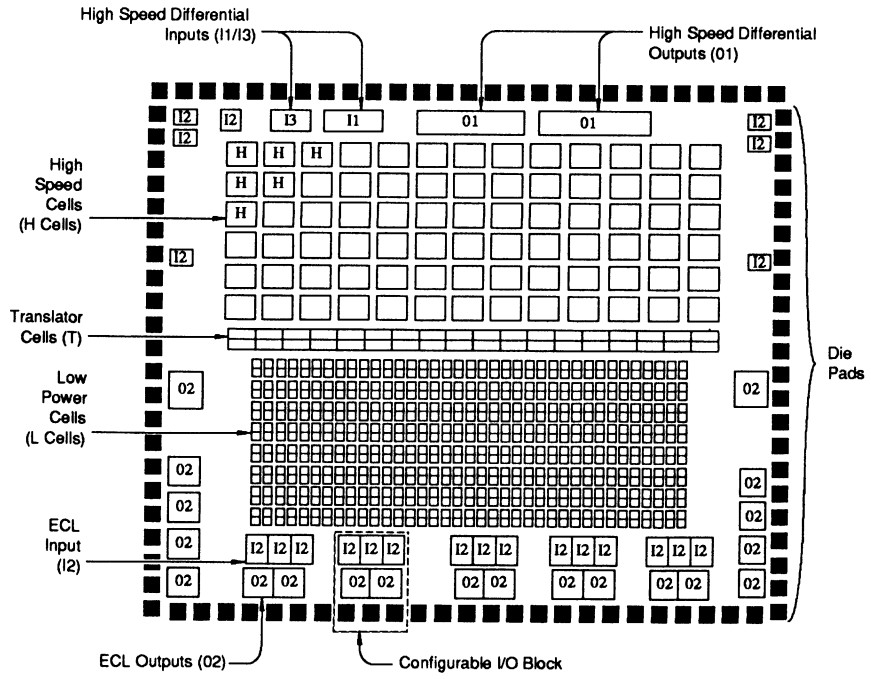


Figure 1: *VSC1500 Gate Array Architecture*

internal architecture of the VSC1500. As seen, the array is divided between two sections. The top section contains ultra high-speed cells capable of flip-flop toggle rates in excess of 2 GHz. This section is typically used for data serialization and de-serialization in communications systems applications. The lower section contains moderate speed cells capable of ultra low-power dissipation. These low power cells are typically used for data processing, storage and manipulation subsequent to de-serialization or prior to serialization.

The SONET Standard

The SONET transmission standard was developed by the American National Standards Institute (ANSI) and the T-1 Committee of the Exchange Carriers Standards Association. Over 200 individual contributions from more than 40 companies helped to complete the SONET specification. This effort establishes, for the first time in history, an international telecommunications protocol for digital optical transmission.

The basic SONET signal, which operates at 51.84Mbit/s, is called Synchronous Transport Signal 1 (STS-1). It is comprised of digital frames, each 125 microseconds long. Each STS-1 signal is divided into two portions, one assigned for transport overhead and another which contains the actual data to be transported. The portion of the frame containing the data is called the Synchronous Payload Envelope (SPE). The SPE can be used to transport a variety of digital data including telecommunications DS3 signals, video data, or a number of lower rate telephone services such as DS1, DS1C or DS2 signals. The transport overhead information is used to maintain the integrity of the digital link and contains bytes associated with identifying frame boundaries, data parity, maintenance, frequency justification, orderwire, channel identification, and user specific functions. Figure 2 illustrates the STS-1 frame which is arranged into 9 rows of 90 bytes each (each row is a sequential 90 byte segment of the STS-1 frame). In each row 87 bytes are reserved for the SPE and 3 bytes are associated with transport overhead.

A primary goal of the SONET standard is to define a synchronous optical hierarchy with sufficient flexibility to carry many different capacity signals. This is accomplished by a byte interleaved multiplexing scheme which results in a family of standard rates and formats which are integer multiples of the basic STS-1

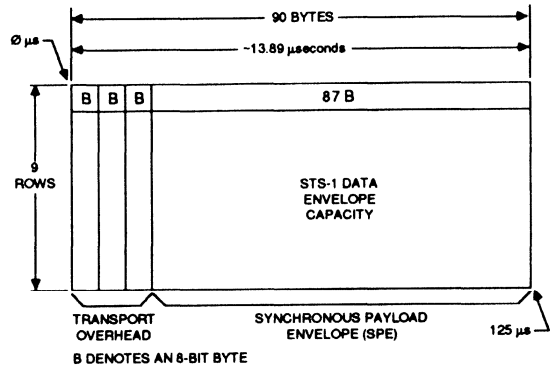


Figure 2: *STS-1 Frame*

rate of 51.84Mbit/s. Since some signals which need to be transported are greater than the basic rate (such as broadband ISDN) a technique of linking several basic signals together to build a transport signal of varying capacity has also been defined. In general, however, higher rate SONET signals are created by interleaving bytes of lower rate SONET signals and modifying the appropriate layer of transport overhead.

The SONET standard only recognizes certain whole number multiples of the basic STS-1 signal as valid higher rate signals. The multiplier values allowed are 1, 3, 9, 12, 18, 24, 36, and 48. Table 1 lists the standard rates and corresponding STS levels which are permissible. The rates which have gained the greatest popularity in the telecommunications community are STS-1, STS-3, STS-12, STS-24 and STS-48. In addition to providing overhead functions, the SONET standard facilitates clock recovery in a digital link by requiring that all bytes in a SONET signal be scrambled by a frame synchronous scrambler of a sequence length of

127 and a generating poynomial of $1 + x^6 + x^7$. Certain overhead bytes such as the ones identifying frame boundaries are exempt from this requirement. The scrambling operation causes the data to be exclusive OR'ed with a pseudo random bit sequence (127 bits long) and thereby provide data transitions in the transmitted signal. These transitions are utilized by clock recovery circuits to extract the clock from the data stream in the receiver. Scrambling is necessary because transition-poor data (all 1's or 0's for example) could cause the clock recovery circuits difficulty in performing their function.

Additional information on the details of the SONET standard can be found in ANSI document T1.105-1988, "Digital Hierarchy Optical Interface Rates and Formats Specification".

Using the VS8010, VS8011, and VS8012

As seen from the previous description, the SONET standard imposes an array of fairly complex requirements on a compliant system. Most of SONET's requirements for composing the basic STS-1 frames can be accomodated in pedestrian CMOS technology because of the relatively low data rates involved. The business of interleaving these basic signals to form the high speed STS-3 to STS-24 frames is much more challenging because it involves the use of a circuit technology which can handle the 155 Mbits/s to 1.24 Gbits/s data rates required.

STS Level	*Line Rate (Mbit/s)*
STS-1	*51.840*
STS-3	*155.520*
STS-9	*466.560*
STS-12	*622.080*
STS-18	*933.120*
STS-24	*1244.160*
STS-36	*1866.240*
STS-48	*2488.320*

Table 1: *Standard SONET Line Rates*

In order to maximize the utility of GaAs technology to the user while minimizing overall system power dissipation, the VS8010 series ICs implement only those functions which necessitate data manipulation at the fast line rate. These functions are bit serialization and de-serialization, and SONET frame recognition and byte alignment. Most other required functions (byte interleaving, overhead byte alteration, data scrambling, etc.) can be accomplished at speeds lower than the line rate, and are more appropriately delegated to an external, low power, gate array. Data scrambling, for example, can quite easily be accomplished at the byte rate with the circuit shown in figure 3. In this parallel scrambler, D1 is assumed to be transmitted first and D8 is assumed to be transmitted last. When ENABLE is LOW the scrambler is off and inputs are equal to outputs. In addition, S1N to S7N are in the state which is the correct initial 8-bit scramble sequence according to the SONET specification. When ENABLE is HIGH the resulting output is a scrambled version of the input and is ready for bit serialization via the VS8010 or VS8011 as appropriate to the application.

For line rates up to STS-3 the external gate array used to implement functions not provided on the VS8010 can be a CMOS device. For line rates between STS-12 and STS-24 Vitesse offers the FURY or LP Series of gate arrays which feature ultra low power dissipation and the ability to interface both with the VS8010 series chips via ECL logic levels and to slower systems utilizing TTL logic levels. These lower power devices can be used since the VS8010 series ICs are capable of reducing the effective data rate by a factor of eight.

In applications where the multiplexer and demultiplexer are co-located (such as a SONET section level node) the VS8010 chip can be used to realize the complete transceiver function. Figure 4 shows a block diagram of a SONET Add-Drop MUX capable of STS-24

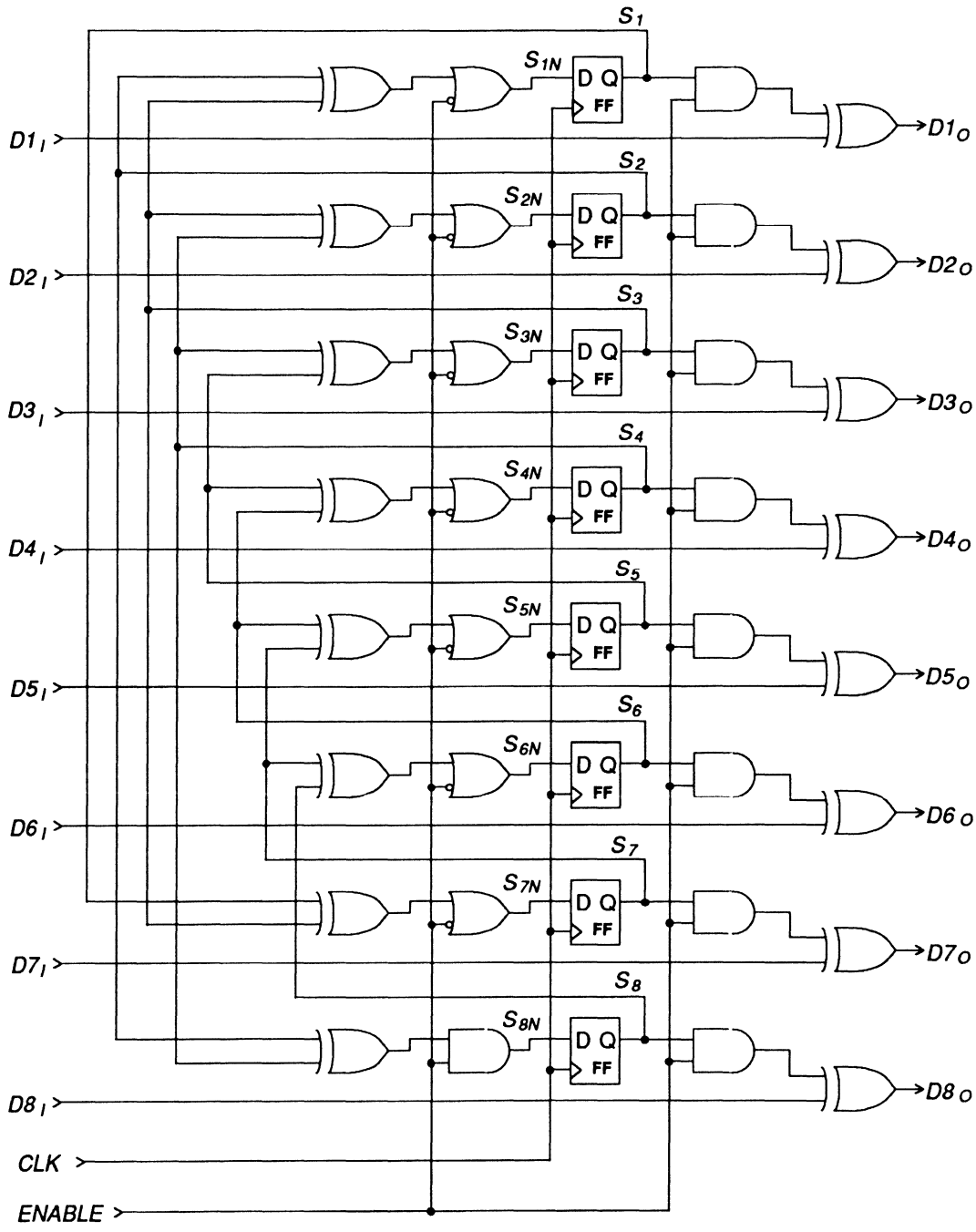


Figure 3: *SONET Parallel Scrambler*

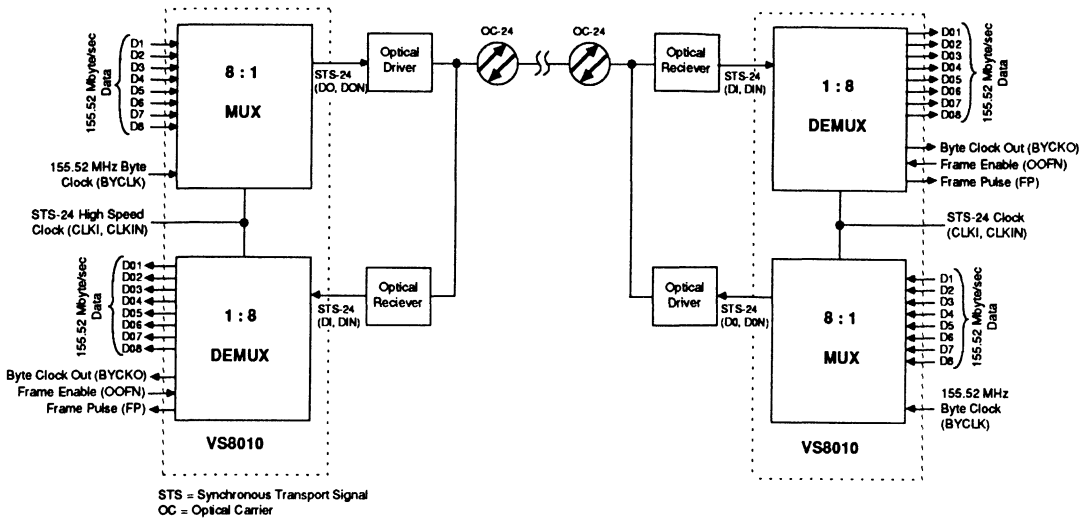
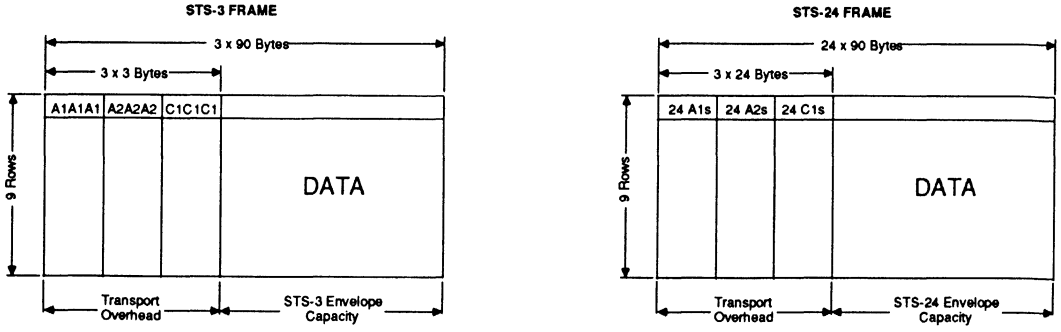


Figure 4: *SONET Section Level Node (STS-24 Line Rate)*

rates. In the event that the multiplexer and demultiplexer functions are not located on the same printed circuit board, a more appropriate configuration would use the VS8011 for the multiplexing function and the VS8012 for the demultiplexing function. The power dissipation of these individual chips is approximately half of the power dissipation of the VS8010 which combines both functions.

Frame Recovery

The primary capability of the VS8010 series ICs which makes them appropriate for SONET applications is their ability to detect the boundary of SONET frames from the framing overhead bytes and to align the subsequently demultiplexed information to the frame boundary. This operation is difficult to implement after information has been demultiplexed and generally requires circuits which operate at the transmission line rate. Since SONET protocol insists on byte wide multiplexing to form higher rate signals, the relative location of overhead information is maintained in any SONET frame. Figure 5 depicts both an STS-3 and an STS-24 frame. Although both frames are 125 microseconds long, the amount of information in the STS-24 frame is much greater due to the higher (1.24 GHz) data rate. Note that in all cases a SONET frame begins with a framing sequence.



A1s & A2s: SONET Framing Sequence
C1s: STS Frame ID

Figure 5: *STS-3 and STS-24 Frames*

STS Level	Line Rate (Mbit/s)	# of A1 Bytes	# of A2 Bytes
STS-3	155.520	3	3
STS-9	466.560	9	9
STS-12	622.080	12	12
STS-18	933.120	18	18
STS-24	1244.160	24	24
STS-48	2488.320	48	48

Table 2: *A1 and A2 Bytes in SONET Frame*

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes (A1 = 11110110 and A2 = 00101000). Table 2 shows the number of A1 and A2 bytes in each SONET frame for different line rates.

Figure 6 shows the functional block diagrams for the VS8010, VS8011 and VS8012 chips. The frame recovery circuits in the VS8010 and VS8012 are enabled on the falling edge of the OOFN input. Once enabled, the frame recovery circuits start looking for the SONET framing sequence. The VS8010 and VS8012 recovery circuits operate from STS-3 to STS-24. The frame recovery circuits look for 3 A1s followed by 3 A2s. The byte clock (BYCKO) and parallel byte data output (DO1-DO8) become invalid on the falling edge of OOFN and become valid when A1 changes to A2. The frame recovery circuits align the received serial data on byte boundaries for demultiplexing by controlling the timing generator. The byte boundary alignment is based on the specific A1 and A2 byte recognition. The falling edge of OOFN must occur at least 4 byte clock periods before A1 changes to A2. The pulse width of OOFN must be at least 1 byte clock period.

The SONET frame detector monitors the incoming data stream. If 3 A1 bytes followed by 3 A2 bytes are detected, a frame confirmation signal is sent off-chip on the output called FP. The rising edge of the FP pulse occurs 2 byte clock periods after A1 changes to A2 on the demultiplexer parallel data outputs. The FP pulse width is one byte clock period. The frame detection circuitry also disables the frame recovery circuits once 3 A1s are followed by 3 A2s. This is done to avoid a false FP signal in the unlikely event that the data payload contains data which is identical to the framing sequence. It is the systems responsibility to reactivate the frame detector every 125 microseconds (the length of a SONET frame). Once the frame is aligned, the FP pulse is generated on every SONET frame. If for any reason the FP pulse disappears on frame boundaries then this signals the system that the frame synchronization is lost. The system then asserts the OOFN input (HIGH to LOW) to recover the system back to a synchronized condition. If the FP pulse does not start up again a link failure may have occurred. Figure 7 shows the timing relationships between important signals in the demultiplexing and frame recovery operation.

Interfaces

Most inputs and outputs on the VS8010 series chips are fully compatible with ECL circuits. Exceptions to this general rule are the

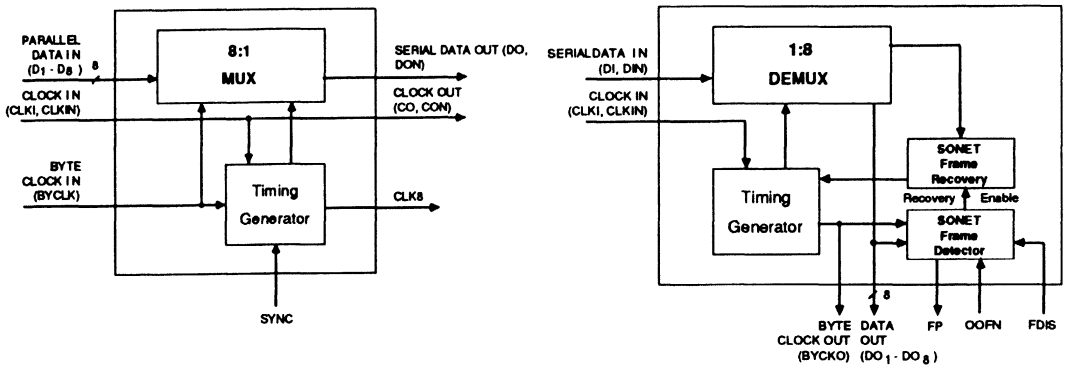


Figure 6: ***a)*** *8:1 Multiplexer and* ***b)*** *1:8 Demultiplexer*

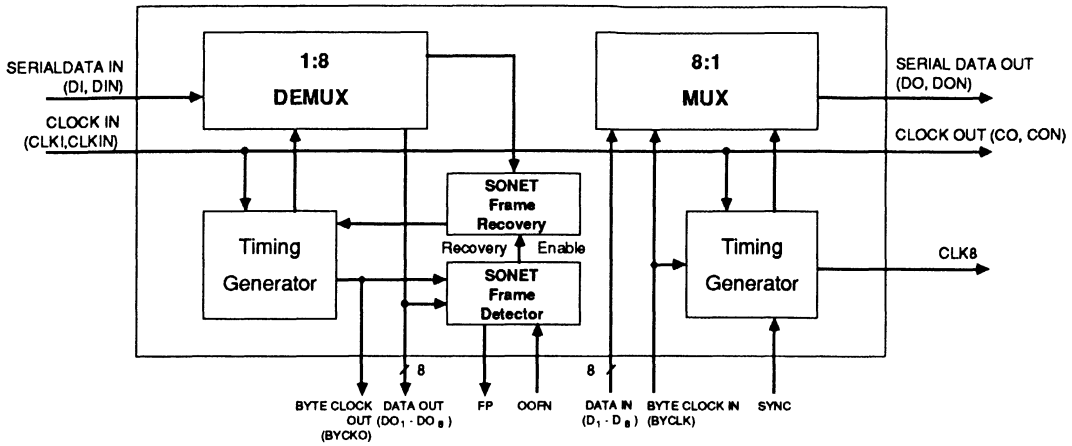
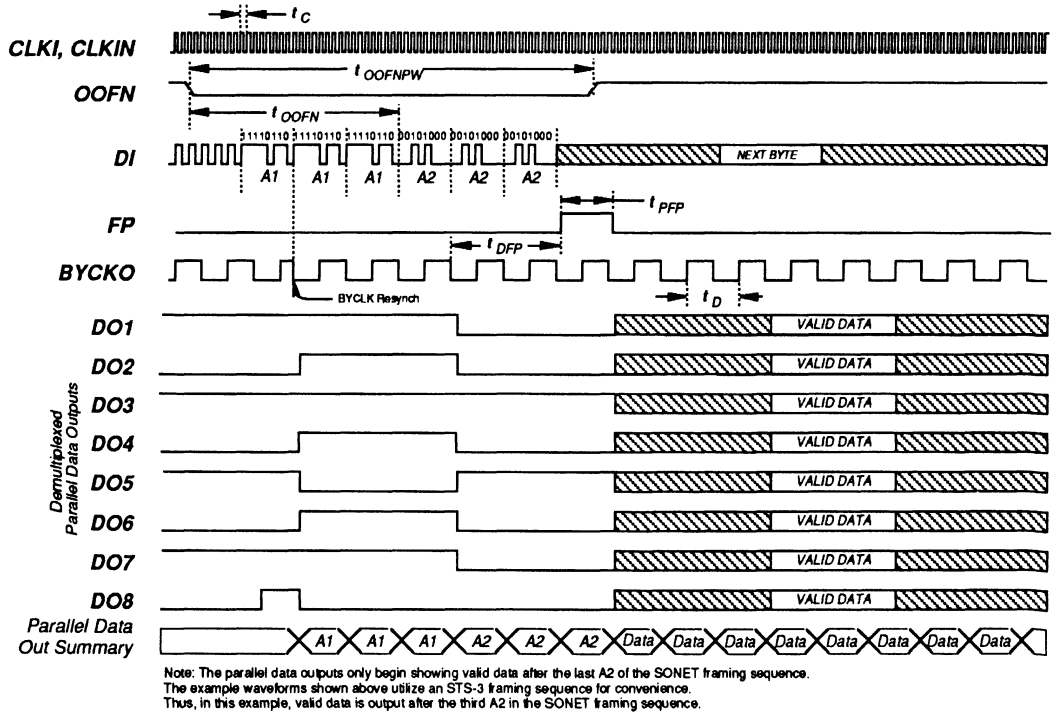


Figure 6: *VS8010 - 8 Bit Mux/Demux with SONET Frame Recovery*

very high speed inputs and outputs assigned to receiving and transmitting serial data and high speed line-rate clock. These interfaces are capable of ac-cepting or transmitting data at rates in excess of 1.5 GHz. Since ECL circuits are not capable of speeds of such magnitude, the high speed I/O of the VS8010 series interfaces with AC coupled signals which could be generated by oscillators or high speed optical receivers/transmitters.

In a typical application the high speed clock (CLKIN) and data (DIN) inputs have an external chip capacitor connected in series between the input and the terminated transmission line carrying the high speed signal. Internal circuitry is responsible for level shifting the AC coupled signal to the appropriate DC levels needed for internal operation. The AC coupled signals



Note: The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence.
The example waveforms shown above utilize an STS-3 framing sequence for convenience.
Thus, in this example, valid data is output after the third A2 in the SONET framing sequence.

Figure 7: *Timing Waveforms for Demultiplexing and Frame Recovery*

Table 3: High Speed Input and Output Levels:
(Over recommended operating conditions. V_{cc} = GND, output load = 50Ω to -2.0V.)

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage	-3.1	-3.0	-2.9	V	Guaranteed HIGH signal for high speed inputs
V_{IL}	Input LOW voltage	-4.1	-4.0	-3.9	V	Guaranteed LOW signal for high speed inputs
V_{REF}	Reference level	—	-3.5	—	V	
V_{OH}	Output HIGH voltage	-1.1	—	-0.7	V	Output load, 50Ω to -2.0 V
V_{OL}	Output LOW voltage	-2.0	—	-1.72	V	Output load, 50Ω to -2.0 V

Notes: 1) A reference generator is built into each high speed input, and these inputs are designed to be AC coupled.
2) If a high speed input is used single-ended, a 100pF capacitor must be connected between the unused high speed or complement input and V_{EE}.
3) Differential high speed outputs must be terminated identically.

should have peak-to-peak amplitudes between 800mV and 1.2V. The DC levels required at these high speed inputs, in the event of DC coupling, are shown in Table 3.

High speed outputs CO, CON and DO, DON on the VS8010 and VS8011 deviate slightly from standard ECL levels. The guaranteed signal levels are also shown in table 3. Note that the peak-to-peak amplitude of these signals is between 620mV and 1.3V.

Support Circuits

In the design of an actual SONET compliant digital optical link, many additional circuits are needed to support the VS8010 series ICs. They include optical transmitters and receivers, clock recovery circuits, high speed clock generation circuits, frame formatting and byte multiplexing circuits. A list of optical transmitters and receivers which are compatible with the VS8010 family are listed below:

7

Optical Transmitters

Company	Model Number	Performance
BT&D	XMT 1100	up to 1.4 Gb/s - 1mW output power
BT&D	XMT 1300	up to 1.4 Gb/s - 200μW output power
PCO	DTX-13-878	up to 878 Mb/s
PCO	DTX-13-678	up to 678 Mb/s
PCO	DTX-13-565	up to 565 Mb/s
PCO	DTX-13-200	up to 200 Mb/s
AT&T	ASTROTEC 1218	up to 1.0 Gb/s
Ortel	3510A	up to 3.0 Gb/s
Ortel	3510B	up to 6.0 Gb/s

Optical Receivers

Company	Model Number	Performance
BT&D	RCV1101-50	up to 50 Mb/s
BT&D	RCV1101-150	up to 150 Mb/s
PCO	DRX-13-878	up to 878 Mb/s
PCO	DRX-13-678	up to 678 Mb/s
PCO	DRX-13-565	up to 565 Mb/s
PCO	DRX-13-200	up to 200 Mb/s
AT&T	ASTROTEC 1306A	up to 1.7 Gb/s
Ortel	3510A	up to 3.0 Gb/s
Ortel	3510B	up to 6.0 Gb/s

Key to Optical Transmitter/Receiver Vendors:

Ortel Corporation
2015 West Chestnut St.
Alhambra, CA 91803

AT&T Technologies
555 Union Blvd.
Allentown, PA 18103

PCO
20200 Sunburst St.
Chatsworth, CA 91311

BT&D
2 Righter Parkway
Wilmington, DE 19083

Metastable Behavior of GaAs DCFL Registers

Application Note 6

Introduction

This application note describes the fundamentals of metastability as well as a method of characterizing metastable behavior. The results of the characterization are applied to a general failure rate formula to predict the reliability of data synchronizers implemented using GaAs DCFL registers.

Metastability Theory

In any system where a single flip-flop (or latch) is used to resolve the timing conflicts between two asynchronous digital circuits, this flip-flop is subject to marginal triggering behavior.[1] In recent years, this general phenomenon has been given the name "metastability". The theory and characterization of metastable behavior is of particular concern in determining the reliability (failure rate) of synchronizer circuits.

A metastable condition can occur when the setup and hold specifications of a register are violated. In Figure 1, Case 1 shows a transition of the asynchronous data which satisfies the setup time requirements of the synchronizing register. A logic "1" is therefore transferred to the register output. Case 2 in Figure 1 shows data which is stable for a sufficient period of time to satisfy the hold time requirements of the register. In Case 3, however, the asynchronous data and the clock transition concurrently, thus causing the output of the register to be indeterminate (neither a logic "1" or a logic "0") for a period of time. The amount of time required for the register output to transition from this indeterminate state to a valid logic state is commonly referred to as the "walk-out" time. The actual window of time where an indeterminate condition can occur is normally much smaller than the specified setup and hold time window for a given flip-flop.

Metastable behavior can also be perceived in terms of its effect on flip-flop delay [2]. As seen in Figure 2, the flip-flop has a normal propagation delay, t_{co}, when the setup time specification is met. As the data input transition moves closer to the clock transition, however, the delay of the flip-flop increases - reaching its maximum value when the clock and data transitions occur simultaneously. As the data input transition moves past the hold time, no output transition occurs.

Perhaps the most important concept in understanding metastable behavior is that the walk-out time is *always* a probabilistic phenomenon. A "maximum" walkout time for a given

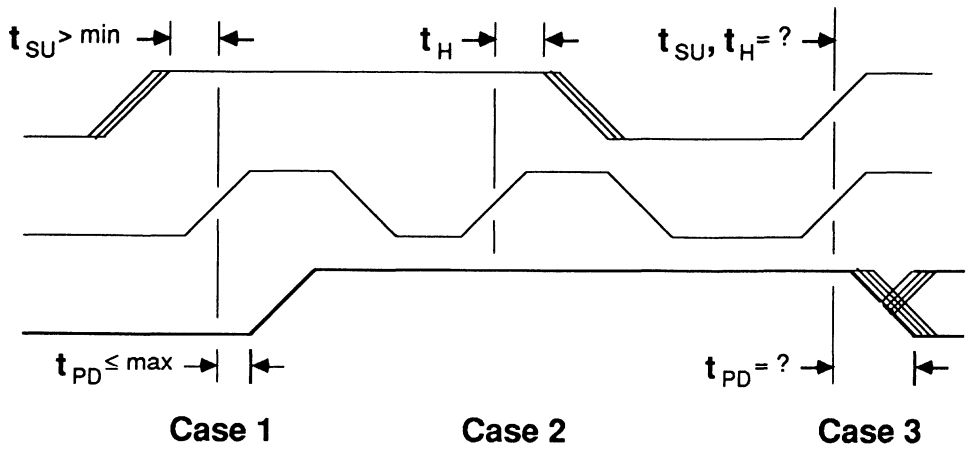


Figure 1: *Data and Clock Relationships for Bi-Stable Elements*

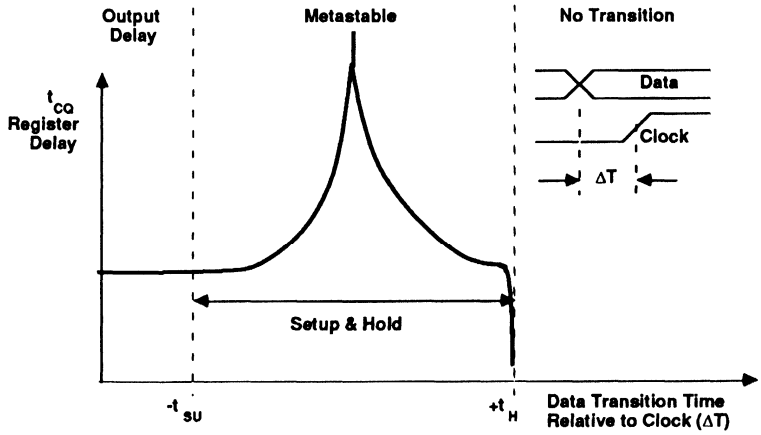


Figure 2: Metastable Delay

register does not exist. Rather, for a certain flip-flop there exists a relationship between a given walk-out time and the probability that this walk-out time will occur. Empirical studies have shown that the mean time between events where the synchronizer flip-flop is still unresolved at time t_w, MTBF(t_w), is: [2,3]

$$MTBF(t_w) = \frac{exp(t_w/K2)}{(K1)(f_{CLK})(f_{DATA})} \qquad (1)$$

for $t_w > h$

where t_w is the time the flip-flop has been allowed to resolve after the clock transition. *K1*, *K2*, and *h* are parameters associated with a particular register and are functions of the circuit design and construction. The total walk-out or indeterminate time can be viewed as two time periods: the amount of time taken for random noise to "push" the output just outside of the metastable state (T_M), and the recovery time (T_R) from time T_M until a valid logic state is achieved.

Metastability Characterization

Metastable behavior can be observed using many different methods. Analog circuit simulators such as SPICE cannot accurately characterize metastable behavior in a bistable element unless an accurate noise model is incorporated into the simulation. Given the random and often complex origins of noise in actual circuits, accurate noise models are quite difficult to create. Metastable behavior can also be observed in the lab using fine resolution delay lines to vary the relationship between clock and data until an indeterminate condition is observed using a triggered oscilloscope. Because metastability is a probabilistic phenomenon, however, it is impossible to obtain the *K1*, *K2*, and *h* constants for a given register using either of the above methods.

The most direct and accurate method of characterizing the metastable behavior of a flip-flop is to construct a synchronizer using that flip-flop and gather statistical data on that flip-flop's failure rate as a function of the settling time allowed. This characterization method readily yields the *K1*, *K2*, and *h* constants necessary to predict synchronizer failure rates. To shorten the duration of the tests, random data transitions can be confined to a small window of time surrounding the active clock transition.

Test Setup

In order to characterize the metastable properties of GaAs DCFL registers, a synchronizer circuit was implemented on a FURY VSC10K gate array. The circuit schematic is shown in Figure 3. In order to simplify the testing, a latch (LLP1U) was used rather than a flip-flop. The LLP1U is an unbuffered DCFL latch. The clock and data

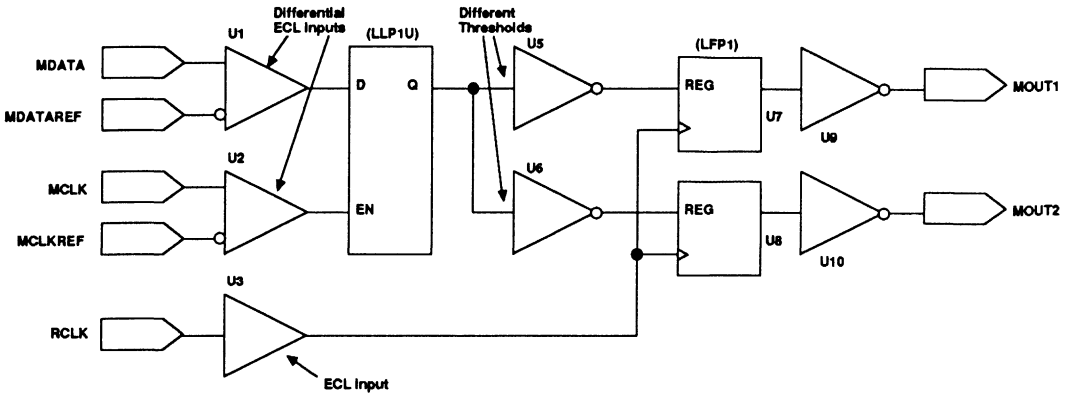


Figure 3: *Metastability Circuit Schematic*

signals are brought onto the chip through differential ECL compatible inputs. The clock (enable) signal was inverted to cause the circuit to latch on a positive clock, again to simplify the test. The output of the latch drives two DCFL inverters, U5 and U6. A difference in switching thresholds between the two inverters is created by using twice the standard D-mode FET width on inverter U5 and twice the E-mode FET width on inverter U6. This threshold window is approximately 130 mV in magnitude centered around the nominal inverter threshold. When the output of the latch is in the indeterminate region, therefore, the output of U5 will be high and the output of U6 will be low. The outputs of U5 and U6 are registered using flip-flops U7 and U8 and are driven off-chip through ECL outputs U9 and U10.

The bench setup shown in Figure 4 was used to conduct the metastability testing. An EH SPG2000 4-channel pulse generator was used to provide the "raw" clock and data signals (MCLK and MDATA) to the latch as well as the RCLK signal to registers U7 and U8. In order to accurately control the relationship between the clock and data signals to the latch, the ECL differential input buffers, U1 and U2), were used as verniers. The MDATAREF signal was set to a fixed voltage to adjust the clock and data signals so that metastable events per unit time were maximized. A triangle waveform was driven onto the MCLKREF pin in order to sweep the latch back and forth through its entire window of metastability. The size of the actual window was determined empirically to be about 15 ps. However, a 350 ps sweep window was chosen (by adjusting the amplitude of the triangle waveform) to ensure that the entire period where metastable events occurred was covered even if the MDATAREF input voltage drifted. Because the slew rate of the MCLK/MDATA signal was set to 0.5 V/ns, a peak-to-peak voltage of 175 mV was used for The register output signals, MOUT1 and MOUT2, drive an off-chip exclusive-OR which in turn drives a 16-bit ECL counter with overflow. For a given test the walkout time, t_w, is controlled by setting the delay between the MCLK and RCLK signals. The time between trials (each trial being a latching edge on MCLK) is set by varying the internal period on the SPG2000 pulse generator. For all of the tests summarized in this document, a period of 100 ns was used which corresponds to a clock rate of 10 MHz. For each part, errors were counted over a specific period of time for various values of walkout time.

All of the testing was performed at room temperature with no air flow applied to the part. A case temperature of 52 ± 2°C was measured for these conditions. A nominal supply voltage of -2.0 Volts was applied to the device under test. Prior to the actual MTBF testing, the output of the latch was observed directly using a sampling oscilloscope to ensure that metastable conditions could be induced by the test setup.

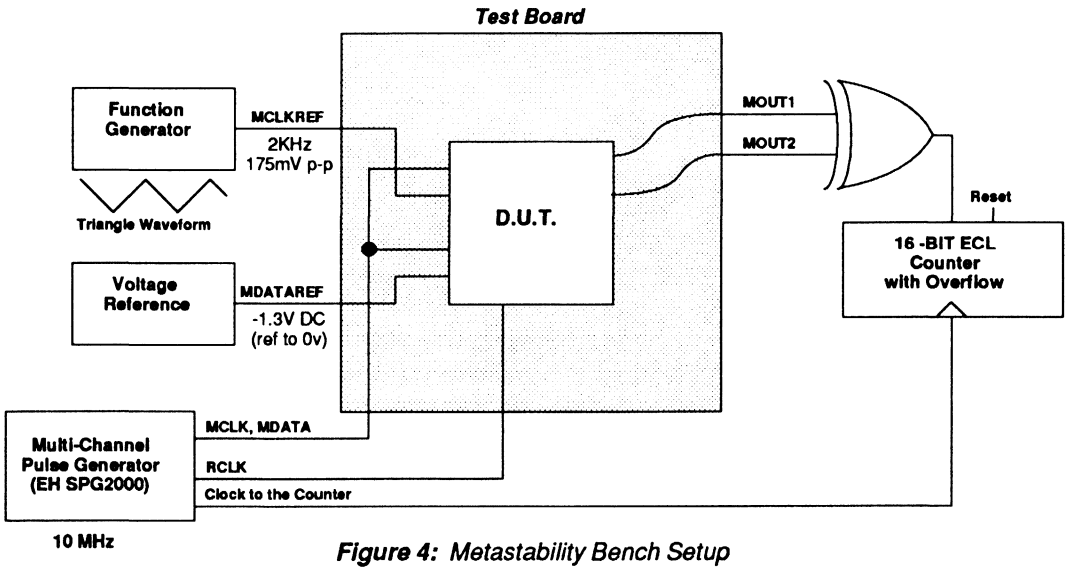


Figure 4: Metastability Bench Setup

Test Results

Figure 5 shows ln(MTBF raw) versus the walkout time. This data is an average of testing done on two devices and is considered to be typical. For both parts, the data taken fit the theoretical model described in equation (1). The value of the experimental constant, *h*, which represents the minimum value of t_w for which equation (1) holds, was not determined but appears to be less than 1 ns. Further testing is required to establish the worst case MTBF for a given walkout time. Vitesse recommends guardbanding the settling time allowed by at least 1 ns to meet the typical MTBF values specified.

The values for *K1* and *K2* are derived from the experimental data using the following relationships:

$$K1 = exp(-ln((f_{CLK})(f_{DATA})) - b) \quad (2)$$

$$K2 = 1/m \quad (3)$$

where:

f_{CLK} = clock frequency to the latch (10 MHz)

f_{DATA} = effective data frequency (1.43 GHz)

m,b = the slope and y-intercept of the linear fit of ln(MTBF) vs. t_w

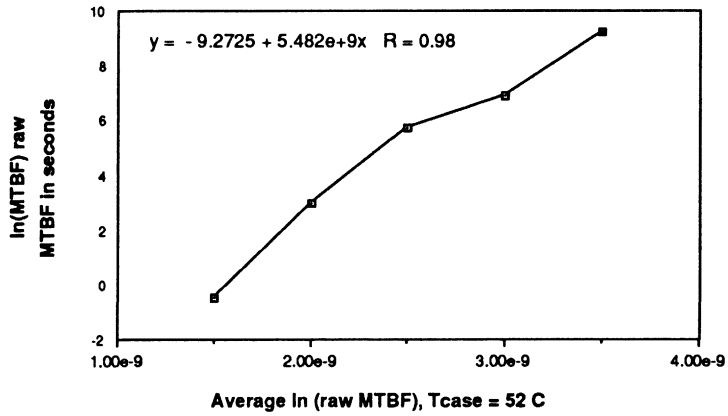


Figure 5: ln(raw MTBF) as a Function of Walkout Time

The effective data rate of 1.43 GHz is achieved by limiting data transitions to the 350 ps sweep window around the clock. Because only a single rising edge occurs in this window, however, the effective data period is twice the sweep window. Using the slope and y-intercept from Figure 5, the values of *K1* and *K2* are:

K1 = 7.44E-13/sec
K2 = 1.82E-10 (dimensionless)

Figure 6 charts the MTBF as a function of walkout time for a data frequency of 100 MHz and a clock frequency of 75 MHz. Data is given for both a GaAs DCFL circuit and a typical ECL register. Table 1 shows the typical MTBF for various combinations of f_{CLK}, f_{DATA}, and t_w. The user should note that these MTBF values are for a single flip-flop. In order to calculate the MTBF for a dual-stage synchronizer, the MTBF of the first stage must be calculated first. This MTBF then becomes the data rate for the next stage when calculating the cumulative MTBF of the two registers in series.

Synchronizer Applications

Knowledge of the metastable behavior of registers in a given technology is crucial to the design of synchronizers. The VMEbus, for example, is an entirely asynchronous bus[2]. Because no timing is specified for bus arbitration signals, decision points such as the bus arbiter, the bus-grant daisy chain, and the interrupt-acknowledge daisy chain must contain synchronizers to resolve timing conflicts. Given that the system clock rate is a known value and the frequency of events to be synchronized can be estimated for the system, the MTBF for the synchronizer can be established based on the MTBF equation for that register. For example, a dual register synchronizer clocked at 100 MHz synchronizing data at 50 MHz will exhibit a mean time between failures of approximately 90 million years, allowing 1 ns for setup time and 1 ns for guardband. If the MTBF for a given amount of settling time is tolerable, a single DCFL register can be used to synchronize random events. For a single register, 100 MHz clock, and 50 MHz data, allowing an additional 5 ns of delay yields a typical MTBF of about 7 years.

Conclusions

Compared with previously published results, initial testing indicates that GaAs DCFL registers are superior to ECL registers in terms of the mean time between failure due to metastable conditions. This result is likely attributable to the fast intrinsic delays of DCFL gates as well as the shorter feedback path inherent in DCFL latches. Past studies show that the trend is for the value of *K2* to be lower for newer and faster technologies [2]. Further testing will allow the variations in metastable

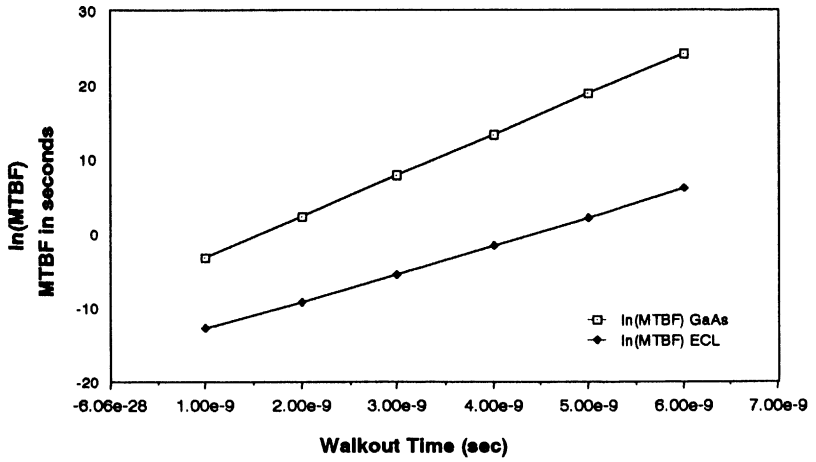


Figure 6: MTBF vs Walkout Time for GaAs and ECL

f_data (Hz)	f_clk (Hz)	t_walk (seconds)	MTBF Expressed in:			
			Seconds	Hours	Days	Years
1E+07	2E+07	4E-08	1.15E+93	3.18E+89	1.33E+88	3.64E+85
2.5E+07	5E+07	1.8E-08	7.69E+39	2.14E+36	8.90E+34	2.44E+32
5E+07	1E+08	8E-09	2.99E+15	8.31E+11	3.46E+10	9.48E+07
5E+07	1E+08	5E-09	2.15E+08	5.99E+04	2.49E+03	6.83E+00
1E+08	2E+08	4.5E-09	3.47E+06	9.65E+02	4.02E+01	1.10E-01
3.3E+07	6.6E+07	1.415E-08	3.04E+30	8.43E+26	3.51E+25	9.63E+22

Table I: *MTBF as a Function of f_{DATA}, f_{CLK}, and Walkout Time*

behavior with respect to process to be determined. Testing over temperature and voltage variations is also scheduled although past research indicates that variations in *K1* and *K2* due to temperature and voltage are minimal compared to variations due to process [2].

References

1 Chaney, Thomas J., "Measured Flip-Flop Responses to Marginal Triggering", *IEEE Transactions on Computers*, Vol. C-32, No. 12, pp. 1207-1209, December 1983.

2 Beaston, John and R. Scott Tetrick, "Designers Confront Metastability in Boards and Busses", *Computer Design*, pp 67-71, March 1, 1986.

3 Chaney, T. J. and F. U. Rosenberger, "Characterization and Scaling of MOS flip-flop Performance in Synchronizer Applications", in *Proc. Conf. Very Large Scale Integration Architecture, Design, Fabrication*, California Instit. Technol., pp. 357-374, 22-24 Jan. 1979.

GaAs DCFL ASIC Design

Application Note 7

Introduction

For several years, Gallium Arsenide ICs have proven extremely useful in high-speed linear applications such as microwave amplifiers and fiber optic drivers. Within the past three years, however, improvements in processing technology coupled with the use of advanced design techniques have made the production of VLSI GaAs integrated circuits a reality. Vitesse Semiconductor Corporation has developed a tightly controlled GaAs enhancement/depletion mode (E/D) process. This process in conjunction with its direct-coupled FET logic (DCFL) design technique has enabled Vitesse to produce and ship ASIC circuits with complexities of over 17,000 gates. The performance of these circuits and the available ECL-compatible I/O structures allow GaAs DCFL ASICs to serve as a viable alternative to ECL gate arrays or standard cells at the system level. This application note describes the similarities and differences in structure and implementation of GaAs DCFL and Bipolar ECL/TTL ASIC devices.

What is Direct-Coupled FET Logic?

Direct-coupled FET logic (DCFL) is a technique used to design logic structures from enhancement and depletion mode FETs. DCFL has been in use since the mid-1970's to build nMOS circuits and is widely recognized for its density and simplicity in the creation of large integrated circuits.

On paper, GaAs DCFL logic looks virtually identical to nMOS with the exception that nMOS uses MOSFETs while GaAs DCFL uses MESFETs. MOSFETs have an oxide insulated gate which prevents the flow of gate current, while MESFETs contain a Schottky barrier diode in the gate-source junction which allows the gate to source current supplied from the previous stage of logic. The gate diode also clamps the internal V_{OH} level to about -1.3 V, or one diode drop above V_{TT}.

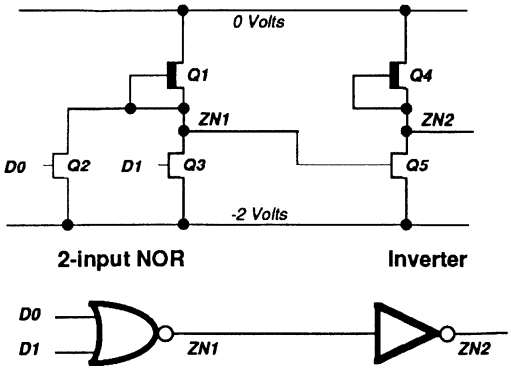


Figure 1: *DCFL 2-input NOR and Inverter*

Figure 1 shows a 2-input NOR driving an inverter. The depletion mode FETs (***Q1*** & ***Q4***) have their gates shorted to their drains and act like current sources. When both ***D0*** and ***D1*** are low, ***Q2*** and ***Q3*** are off, allowing ***ZN1*** to rise and turn on ***Q5***. The current from ***Q1*** in this case will flow through the gate of ***Q5***. If either ***D0*** or ***D1*** are pulled high, the ***Q1*** current is shunted through ***Q2*** and/or ***Q3***, pulling ***ZN1*** low.

DCFL Features

The key advantages of DCFL are circuit simplicity and the ability to switch very quickly using a small supply voltage. The 2-input NOR gate shown in figure 1, uses only three transistors (resistors are not necessary). GaAs DCFL can operate reliably on a 1.1 V power supply, in contrast to bipolar ECL which requires either 4.5 or 5.2 V. Unlike ECL, no internal reference voltages are needed for GaAs DCFL circuits. All logic switches around the enhancement-mode FET threshold (about 250 mV above the source voltage, V_{TT}).
On the flip side, however, GaAs DCFL does not allow the use of series-gated structures, wire-ORs, or collector-dotting (all features of ECL). This is offset by the higher circuit density and corresponding shorter device interconnec-tion lengths found in GaAs DCFL. Virtually all logic structures which have been created for Vitesse ASIC products ars constructed from simple

inverters or two to four input NOR gates. Figure 2 depicts a full adder macro implemented in GaAs DCFL. The logic portion of this macro is built from three 2-input NORs, five 3-input NORs, and one 4-input NOR. Vitesse incorporates a proprietary buffer on the outputs which effectively drive large capacitive loads with very little skew between the rising and falling edges. Table 1 is a comparison of the GaAs DCFL full adder macro with an equivalent version implemented in silicon bipolar ECL technology. Note that the GaAs DCFL version has a significantly shorter propagation delay, dissipates less than 30% of the power and uses only 70% of the space needed by its silicon counterpart.

Buffering Tradeoffs

Many ECL ASIC products allow for a tradeoff between speed and power. This is generally accomplished by allowing the designer to select different switch and emitter follower current values by paralleling resistors using the metal personalization. Generally, the resistors necessary for at least two different speed/power versions of many functions are included in the basic cell. In GaAs DCFL, however, the tradeoffs involved in buffering are somewhat different. In Vitesse's FURY Series of gate arrays, internal macrocells can have unbuffered, 1x drive, or 2x drive outputs. The tradeoffs involved with this choice of buffering involve speed, power, and density. Moreover, the speed/power versus density tradeoffs will vary depending on the complexity of the macro function. In general, the presence (or absence) of buffering affects the intrinsic delay of the macro very little. Buffering will increase the driving ability of the macro output in terms of both DC drive limitations and AC performance. On the other hand, buffering requires additional depletion and enhancement mode devices which could otherwise be used for logic and also consumes additional power. The more complex the macro function, the less the price paid for the buffer in terms of percentage area and power. Figures 3 and 4 depict the buffering tradeoffs for a 4-input NOR and a D flip flop in the FURY Series macrocell library.

Parameter	GaAs DCFL	Silicon ECL
$A/B \rightarrow SUM$	836 ps	1125 ps
$C_{in} \rightarrow C_{out}$	587 ps	1338 ps
Power (typ)	4.8 mW	16.58 mW
Area	21236 μm^2	31750 μm^2

Table 1: *GaAs DCFL vs. Silicon ECL: Full Adder Macro Comparison*

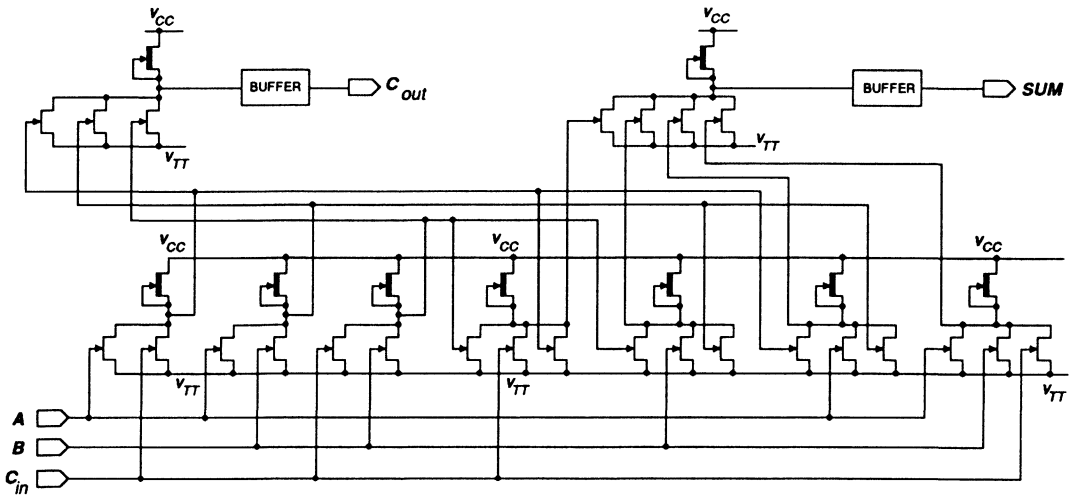


Figure 2: *Full Adder Implemented in GaAs DCFL*

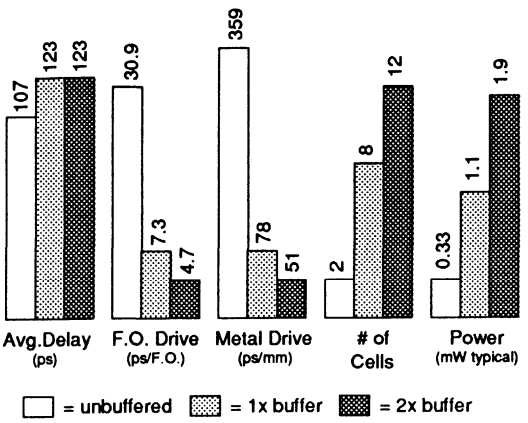


Figure 3: *Buffering Tradeoffs for a 4-input NOR*

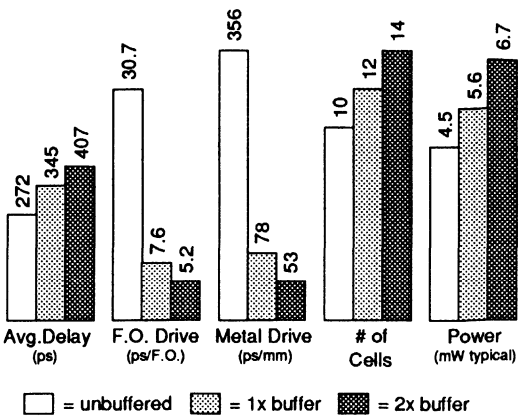


Figure 4: *Buffering Tradoffs for a D Flip-Flop*

Gate Array Architecture

Like most third-generation ECL gate arrays, the Vitesse FURY Series of gate arrays employ a channeled architecture. Metal 1 is used to route within macrocells and in the vertical channels between macrocell columns reserved for routing. Metal 2 channels run horizontally over the entire core area. A third layer of metalization is used for fixed power and ground distribution in the macrocell columns. Figure 5 shows the layout of the FURY VSC15K array. The I/O ring contains 96 input-only buffers on the sides of the array and 100 input/output buffers on the top and bottom for a total of 196 I/O pads. A D-latch or buffer can be imple-

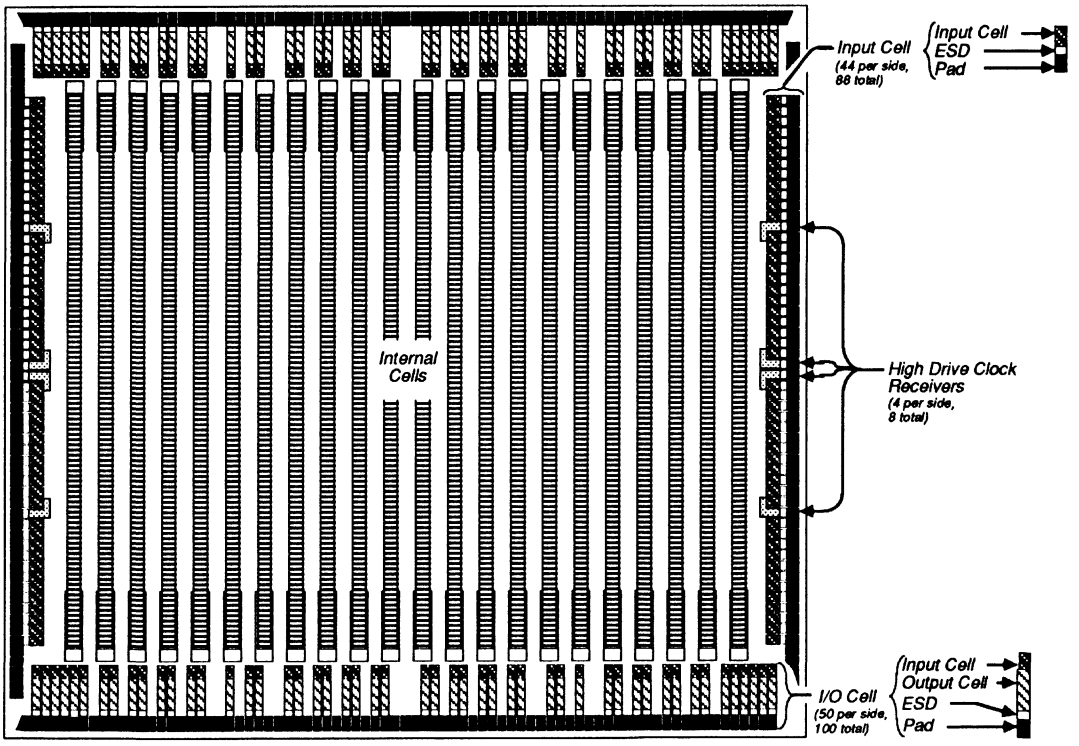


Figure 5: *VSC15K Layout*

mented in the input-only cells and a D-flip flop or a 2 or 3-input OR/NOR gate may be placed in the output cell structure. In addition, each FURY array contains a small number of high-drive input cells which are used for distributing large fanout signals, such as clocks, to local buffers in different areas of the core.

Each cell column in the core is composed of a large number of "slices" (192 in the case of the VSC15K). A slice consists of four cells in a 2 by 2 configuration (see figure 7). A cell is equivalent to an unbuffered 2-input NOR (two enhancement-mode FETs and one depletion-mode FET). The minimum addressable unit (MAU) in a FURY array is two cells (six FETs). By contrast, the typical ECL gate array MAU contains 10 to 19 transistors and an equal number of resistors. The finer granularity of the FURY MAU minimizes the number of wasted transistors in a given macrocell implementation allowing for virtually 100% use of the core cells.

To the IC designer, a Vitesse GaAs DCFL gate array appears much the same as its present ECL counterpart. Both have internal and I/O macrocells and both generally use channeled architectures with two layers of user metal and one layer of power/ground metal.

Standard Cell Architecture

The benefits of standard cells (where all mask layers are customized) over a gate array (where only the metal interconnects are personalized) can be summarized in terms of flexibility. Vitesse's VCB50K GaAs Standard Cells offer several advantages over gate arrays: superior density, the ability to include megacell functions (RAM, ROM, ALU, etc.), and the option of using alternate logic families or structures such as source-coupled FET logic (SCFL) or transfer gate flip-flops which offer superior speed performance to DCFL.

Superior Density

The general structure of Vitesse's VCB50K Standard Cell product is similar to that of a chan-neled gate array at first glance. Figure 6 shows several cells in the core area of a VCB50K Standard Cell implementation. Four

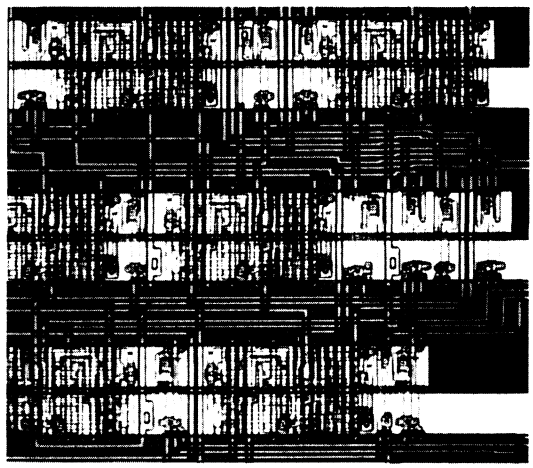
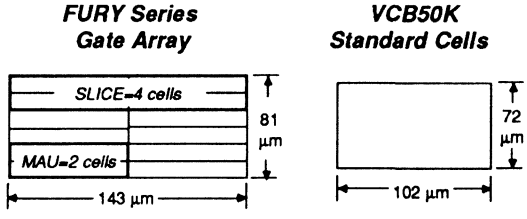


Figure 6: Section of VCB50K Core

layers of metal interconnection are used (gate metal and three layers of global metal). Gate metal and metal 1 are used for cell intracon-nections, metal 1 and 2 are used for inter-cell routing, and metal 3 is reserved for power and ground distribution.

Standard cells are denser because gate metal can be used for routing within cells and the channel area is decreased (channels are customized for a given amount of intercon-nection). This is demonstrated in figure 7 which compares the D flip-flop from the FURY Series Macro Library with an equivalent one from the VCB50K Standard Cell Library. The standard



Parameter		FURY	VCB50K
Area		11583 µm²	7344 µm²
Power		3.9 mW (typ)	4.3 mW (typ)
Delay	(rising)	428 ps	399 ps
	(falling)	540 ps	392 ps

Conditions: Commercial temperature range, worst case process and power supply variation, fanout = 3

Figure 7: D Flip-Flop Comparison FURY vs. VCB50K

cell version is smaller and faster but consumes slightly more power than the FURY macrocell.

RAM/ROM Megacells

As with ECL standard cell architectures, the VCB50K Standard Cells allow for the inclusion of custom, hand-packed "megacell" blocks. The blocks offered in the VCB50K library include a 4-bit microprocessor slice, a carry look-ahead generator, a microprogram sequencer, SRAM, and ROM cells. Unlike newer ECL standard cell technologies which use BiCMOS for the implementation of dense RAM, the VCB50K uses the same GaAs E/D process and design rules for RAM and ROM blocks that are used for standard DCFL logic. Vitesse is currently using this process to produce the VS12G478, a 2Kx2 5ns SRAM (see figure 8). The VCB50K library contains several standard static RAM megacells in blocks up to 1K x 2.

SCFL Logic

In addition to DCFL logic, the VCB50K standard cell family also contains several source-coupled FET logic (SCFL) macrocells. These cells use only depletion-mode FETs in a differential CML structure. This family is optimized for clock frequencies up to 3.5GHz. SCFL cells are much larger and consume much more power than their DCFL counterparts, but are indispensable for the implementation of circuits such as the VS8004 and VS8005, 2.5Gb/s Mux and Demux from Vitesse.

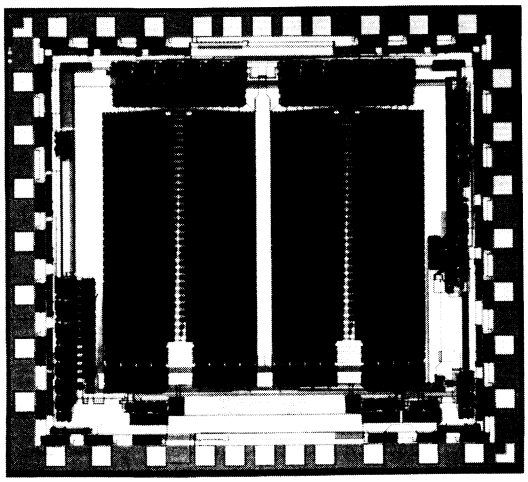


Figure 8: VS12G478 2K 5 ns SRAM

System Considerations

At the system level (i.e., looking at a packaged part as a black box), Vitesse GaAs ASICs are virtually identical to ECL ASICs. ECL I/O buffers as well as TTL buffers are supported on all FURY and VCB50K ASIC products. In implementing a board design which includes a Vitesse ASIC, however, the designer should be aware of ECL I/O differences, power supply requirements, and the availability of GaAs I/O as an interface alternative.

ECL I/O

Vitesse ASICs support ECL 100K input and output levels. Unlike standard ECL 100K, however, the GaAs V_{OL} min is always equal to V_{TT} because the ECL outputs are cutoff in the low state. This is not a problem in digital applications, but may necessitate the use of a higher V_{TT} (approximately -1.7 Volts) when driving a DAC because of potential analog feed-through problems associated with the larger input swings. Also, the -2.0 Volt supply must be controlled to ±5% to ensure that adequate noise margins are maintained using the internal V_{BB} reference generator. If such regulation is not feasible, or if the design must receive 10KH levels (which vary with temperature), then an external V_{BB} reference should be supplied.

Power Supply Considerations

Nearly all Vitesse ASICs use -2 V as the primary supply voltage. In fact, for an ECL-only interface, -2 V is the only supply required. Although the power dissipated by GaAs DCFL circuits is relatively small, the -2 V regulator must be capable of supplying a large amount of current (up to 4 Amps in the case of a fully utilized VSC15K gate array).

The use of SCFL in the HS Series gate arrays and the VCB50K Standard Cell products requires a -5.2 Volt supply, and a +5 V supply is required in applications where TTL interface is necessary.

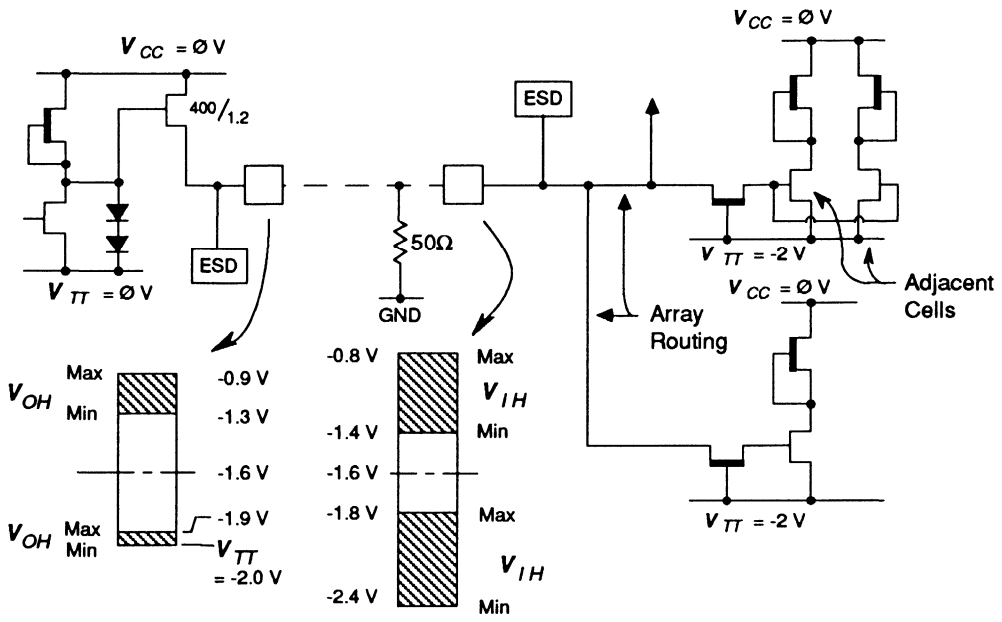


***Figure 9:** GaAs I/O Interface*

GaAs I/O

In addition to standard ECL and TTL buffers, FURY gate arrays and VCB50K cell-based ICs support I/O buffers which communicate with internal DCFL voltage levels. Figure 9 shows a GaAs output driving the GaAs input on another IC. The primary advantage of this I/O scheme is the elimination of the delay and power dissipation associated with logic level translations (ECL or TTL). The GaAs output of one chip drives the internal logic of the receiving chip directly. A pass transistor is used to limit the gate current at the DCFL input.

Conclusion

Though the internal logic structures and raw materials used to construct GaAs DCFL ASICs are somewhat different from those used to build ECL ASICs, the two technologies are virtually identical at the system level. The density and performance of GaAs DCFL ASICs make them attractive alternatives to ECL ASICs in many systems. With the advent of the VCB50K standard cell family, the system designer now has the flexibility to more fully reap the benefits of GaAs DCFL technology. The major advantage of GaAs DCFL technology is the ability to produce ASIC devices which offer better density and performance than ECL while dissipating only 1/4 to 1/5 of the power.

Generating an External ECL Input Reference

Application Note 8

Introduction

The use of multiple ECL (or ECL-compatible GaAs) ASIC devices on a circuit board may require the addition of an externally generated ECL input reference voltage (V_{BB}). Providing this reference ensures that the input receivers of the ECL devices will all switch at the same threshold voltage independent of power supply or temperature variations.

This application note describes a method for providing an external ECL input reference (-1.32 Volts) from a standard -2.0 Volt ECL supply using an adjustable micropower voltage reference and three resistors.

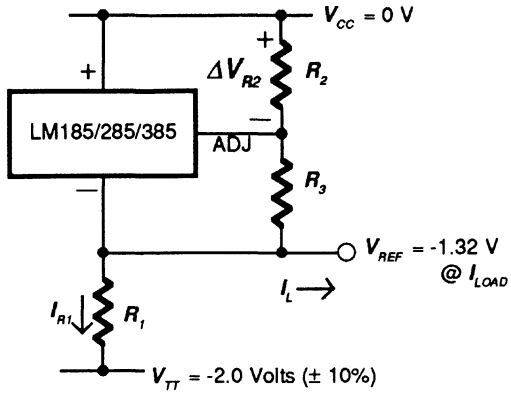


Figure 2: *ECL Reference Circuit*

Reference Circuit Description

The reference circuit employs three resistors and an LM185, LM285, or LM385, which are 3-terminal adjustable band-gap voltage reference devices available from National Semiconductor Corporation. The LM185 is rated for operation over a -55°C to 125°C temperature range, while the LM285 is rated from -40°C to 85°C and the LM385, from 0°C to 70°C. A block diagram of the LM185/285/385 is shown in Figure 1. The circuit shown in Figure 2 is used to create the voltage reference.

The reference circuit shown in Figure 2 uses V_{TT} and V_{CC} as external voltages to produce the reference voltage, V_{REF}. In order to create a reference which can be used with Vitesse ECL-compatible ASIC parts, the values for R_1, R_2, and R_3 must be chosen under the following operating conditions:

- Supply Voltage, *(V_{TT})*
  -2.0 Volts (± 10 %)
- Current through LM185/285/385 from + to —, *(I_D)*
  0.10 to 20 mA
- ADJ Current through LM185/285/385, *(I_A)*
  ≤ 10 nA (guaranteed by LM185/285/385 specs)
- Current to each Vitesse ECL compatible input cell from V_{REF}, *(I_{Input})*
  ≤ 5 μA
- Potential between V_{CC} and ADJ, *(ΔV_{R2})*
  1.24 Volts (reference voltage produced by the LM385)

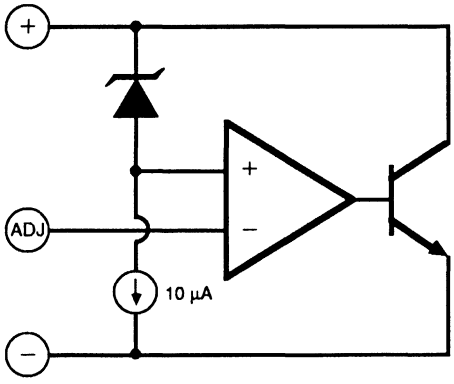


Figure 1: *LM185/285/385 Block Diagram*

The values for R_2 and R_3 must satisfy the following condition:

$$V_{REF} = -1.24 \left(\frac{R_3}{R_2} + 1\right) \qquad [1]$$

By equation [1], the following commonly available resistor values can be used for R_2 and R_3 to create a -1.32 Volt ± 10mV reference:

R_2 = 16K Ω
R_3 = 1K Ω

The stability of V_{REF} depends on the tolerances of these two resistors. If k is the maximum normalized value and p is the minimum normalized value of the resistors R_2 and R_3 expressed as decimals, then the variation in V_{REF} is given by the following equation:

$$\Delta V_{REF} = \frac{\frac{R_3}{R_2}\left(\frac{k}{p} - 1\right)}{\frac{R_3}{R_2} + 1} \qquad [2]$$

Assuming that the resistors have a 5% tolerance and substituting values into the equation, we can then solve the equation:

$$\Delta V_{REF} = \frac{\frac{1K\Omega}{16K\Omega}\left(\frac{1.05}{0.95} - 1\right)}{\frac{1K\Omega}{16K\Omega} + 1} \qquad [3]$$

ΔV_{REF} = 0.6% or ~8mV

Although use of 5% resistors gives a tight V_{REF}, it is advisable to use 1% metal film resistors instead of the commonly available 5% carbon composition resistors to minimize aging effects and to compensate for the tolerance on the 1.24 Volt band-gap reference voltage. R_1 determines the no load regulator current. Assuming worst case power supply and 175μA total regulator current, then:

$$R_1 = \frac{1.8\text{-}1.32}{175\mu A} = 2.7\,k\Omega$$

Since the regulator can source up to 20mA, as many as 4000 Vitesse ECL inputs can be supported. Thus, a single regulator circuit, as shown in Figure 3, can be used on a circuit board to supply ECL input reference for many

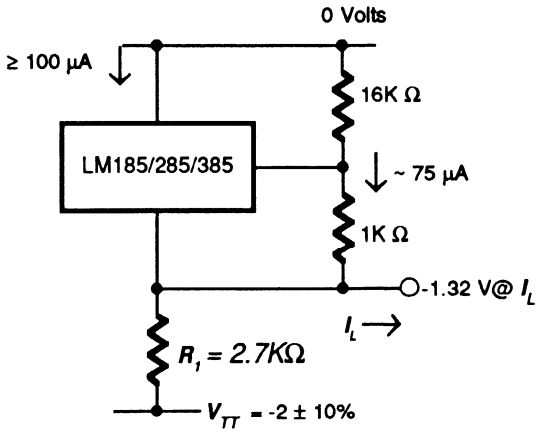


Figure 3: Implementation of Reference Circuit

Vitesse IC's. A typical Vitesse compatible external V_{REF} pad is shown in Figure 4. The exact number of IC's is dependent upon the number of ECL inputs per IC. The load current per input cell is ≤ 5μA, with an additional 100μA ESD diode leakage current per chip. For example, if 3 ASIC devices with 40 inputs each are serviced by the external V_{REF} circuit, then:

I_L = (3x40x5μA) + (3x100μA)
= 900μA

When more than 40 inputs are connected to the reference, the value of the bleeder resistor R_1 becomes relatively unimportant and, for example, can be made equal to R_2 (16KΩ) in order to reduce parts inventory.

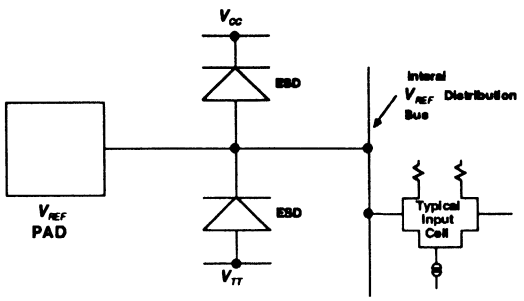


Figure 4: Typical Vitesse External V_{REF} Pad

Notes

1. In order to use this reference generation scheme, the Vitesse ASIC product (gate array or standard cell) must be specified with an external ECL reference.

2. Vitesse recommends the use of a 0.001 to 0.01 μF bypass capacitor at the reference input pin of each array. Refer to the design manual for the particular ASIC product for the location of the input reference pins.

3. Care must be taken to account for the effect of IR drop in the reference net on the PC board.

50 MHz Cache Controller for the 80486 Using the PLR2KT

Application Note 9

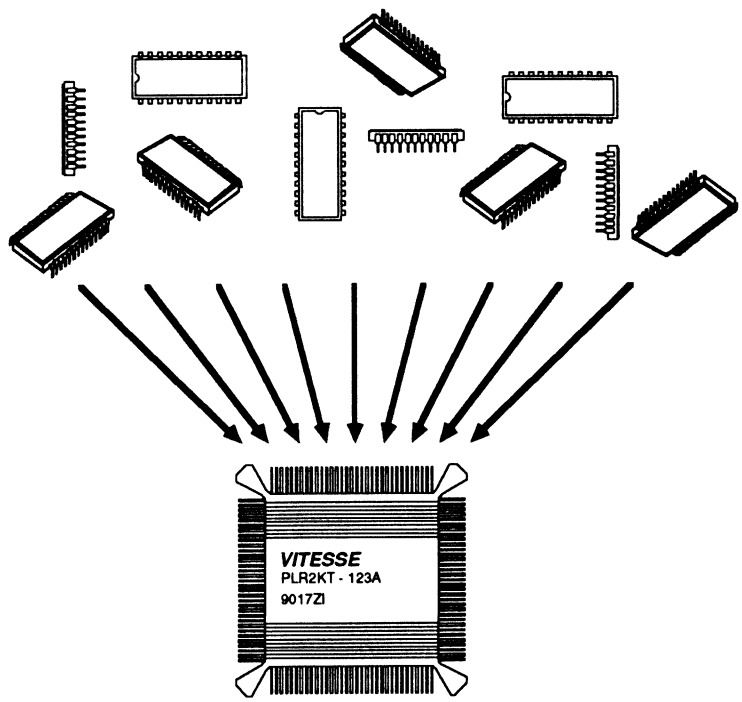
Introduction

This application note describes a write-through cache controller implemented in the PLR2KT gate array from Vitesse Semiconductor. This controller is designed for Intel's 80486 microprocessor with system clock frequencies up to and including 50 MHz. A single level of write posting is shown which, along with a page mode DRAM controller, allows writes and reads from the processor to be handled at a pipelined rate of zero-wait states.

The i486 microprocessor has brought workstation performance levels to personal computer systems. While currently shipping at 25 MHz, 33 MHz units are expected to ship in the second quarter of 1990, and it is anticipated that 40 and 50 MHz units will follow.

The i486 includes a 8 Kbyte, four-way, set associative, write-through cache on-board. While this cache is adequate for MS-DOS applications, its effectiveness diminishes for multitasking operating systems such as UNIX, OS/2, and Novell NETware™. Most system designers have added 128 to 256 Kbyte secondary caches to improve performance for these operating systems. It should be noted that, even assuming only an 80% hit rate, the on-board cache greatly reduces the number of read cycles which appear on the output of the i486. Because of this, approximately 75% of the cycles on the outside of the i486 are write cycles. It is very important, therefore, to optimize the secondary cache controller for these write cycles.

The PLR2KT from Vitesse Semiconductor is an excellent choice for implementing cache and DRAM controllers for up to and including 50 MHz i486 systems. The PLR2KT is a high performance, 2400 gate, GaAs gate array which is compatible with +5 V TTL or CMOS systems. The device is packaged in a 132-pin Metal Quad flatpack and provides up to 92 I/O signal pins (52 of which can be configured as outputs). With input to output delays as low as 6 ns and internal gate delays of 177 ps the PLR2KT is an ideal replacement for high speed (5 to 10 ns) programmable logic and TTL devices. Actual designs have demonstrated that up to 17 PLD's can be replaced by the PLR2KT with significant power, cost, board area, and reliability improvements.



Cache Organizations

Several approaches to cache design are possible with the PLR2KT. Two of these approaches, write-through and write-back, are described below:

1) Write-Through Cache

With this type of cache, a read request that isn't currently in the cache is read from main memory, given to the processor, and placed into the cache at the same time. If a write request occurs to a location that is already in the cache it is termed a write hit and the information is written into the cache. This information is also immediately dispatched to the memory usually with at least a single level of write posting. Multiple levels of write posting are also possible. During DMA (direct memory access) and bus master cycles, the cache must look out for write requests to locations which are currently located within the cache and either write the new data in the cache or invalidate the cache location.

Historically, the write-through cache was perceived as having the disadvantage that all write requests must result in a write command to main memory. However, if the memory subsystem can handle these writes in a few clock cycles, this will not be a limitation.

Since the i486 provides an on-board, four-way, set associative cache, the secondary cache need only be direct-mapped. This is because the i486 cache will effectively eliminate the read thrashing usually found in direct-mapped caches and writes will go through the cache anyway.

2) Write-Back Cache

With caches of this type, write requests result in data which is written directly to the cache but not immediately into DRAM. Locations which have been written in the cache but not to DRAM are marked "dirty". If a read miss occurs at a "dirty" location, the information at this location must first be removed and written into DRAM, then the new information can be read. When a write miss to a "dirty" location occurs, the "dirty" data must first be written to DRAM, then the new data is read to make the cache line or block valid. Afterwards, the new data may be written into cache. During DMA and bus master cycles the cache controller must watch for write requests to locations within the cache and either write the data on hits or invalidate the location. On DMA or bus master reads the cache controller must watch for read hits to "dirty" locations. When a read is found at a "dirty" location, the cache must provide this data and keep the DRAM from providing the data since the cache contains the only valid copy.

The advantage of a write-back cache is that many reads and writes may occur with no DRAM cycles required. As more cycles occur to "dirty" locations, the amount of DRAM activity will increase.

Another supposed advantage of write-back caches is that they can support multi-processor designs. This is because each processor can utilize its own cache, resulting in lower bandwidth requirements on the shared memory. At higher system speeds, this advantage is difficult to achieve because the cache tag and data RAMs must be made available to snoop information for other processor reads and writes, and the i486 address bus must be made available to invalidate locations within the i486 on writes.

A disadvantage of the write-back cache is that in the EISA, Micro Channel, or AT bus, cache coherency is not directly supported. This means that a write-back cache can only cache memory which it can disable when DMA or bus masters read "dirty" locations. Because of this, only the memory on the system board can be cached.

Also, if memory writes can be written out to the memory subsystem as fast as they can be written into the cache, then the write-back cache may actually be a disadvantage because information in a "dirty" location must be written to memory before the read can occur. This slows down the read and does not result in an advantage on a write.

Write-Through Cache Controller

While this application note only presents one type of cache controller, the PLR2KT is well-suited for virtually any approach due to its high speed and large pin count.

Figure 1 shows a i486 system with a PLR2KT implemented as a write-through cache controller and a single level write poster. In this implementation, a direct-mapped cache of either 128 Kbytes or 256 Kbytes is provided. The tag directory is implemented with four CY7C161-15 16K X 4 SRAMs (Cypress Semiconductor). This provides the tags required for both a 128K or a 256K byte cache. The use of large off-chip SRAMs for the tag directory results in small, manageable cache block sizes. This is one of the major advantages of this approach. The data RAMs are implemented with the new IDT 71589-15 Synchronous CacheRAMs (Integrated Device Technology, Inc.), which are specifically designed for the i486. Similar devices are

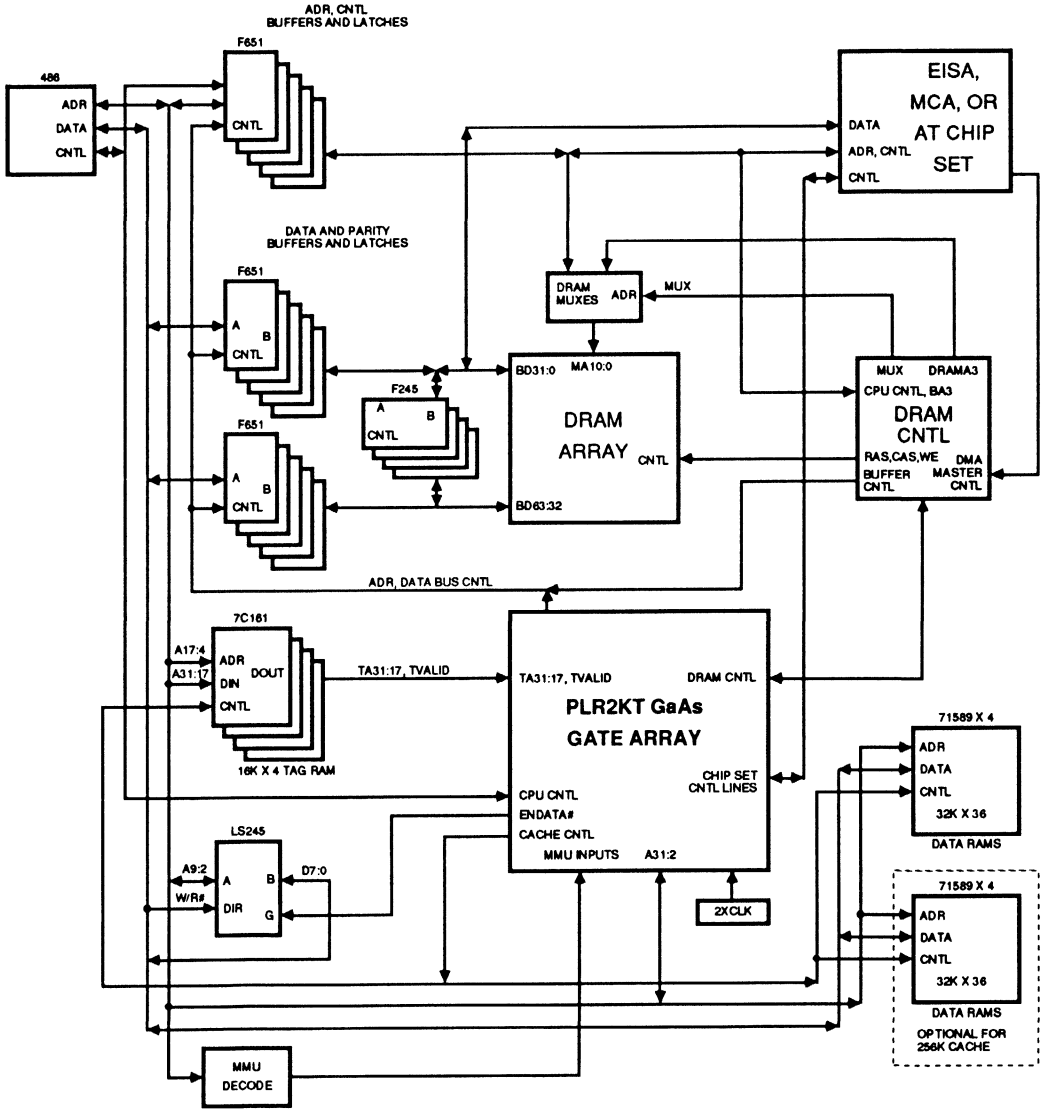


***Figure 1:** 486 System Block Diagram*

anticipated from Micron Technology, Motorola, and Sony. Four of the IDT 71589s are required for a 128K byte cache, and eight for a 256K byte cache. A single level of write posting is provided by using F651 Buffer/Latches (similar to a 646 but with independent output enables instead of enable and direction controls) on the address and data/parity busses.

Although some main memory decoding is done in the cache controller chip, the actual DRAM signals are generated in another PLR2KT personalized as a DRAM controller. The DRAM control chip provides control of two banks of 64 bit wide DRAM. This allows support of up to 64 Mbyte of DRAM using 4 Mbyte DRAM devices. 64 bit wide DRAM is used to support the burst mode read capability of the i486.

The MMU (memory management unit) shown in Figure 1 is used to provide cache enable, write protect and DRAM bank select region infor-mation. It can be implemented using the CY7C161-15 16K X 4 SRAM. This could provide information on 16K boundaries within the first 256 Mbyte of address space. Other implementations are possible but will not be covered here.

Figure 2 is a block diagram of the cache controller implementation of the PLR2KT. Tables 1 A-G give a description and summary of the pins required for this implementation. A gate estimate shows that the design fits comfortably in the 2400 gates available on the PLR2KT. A summary of this estimate is given in Table 2.

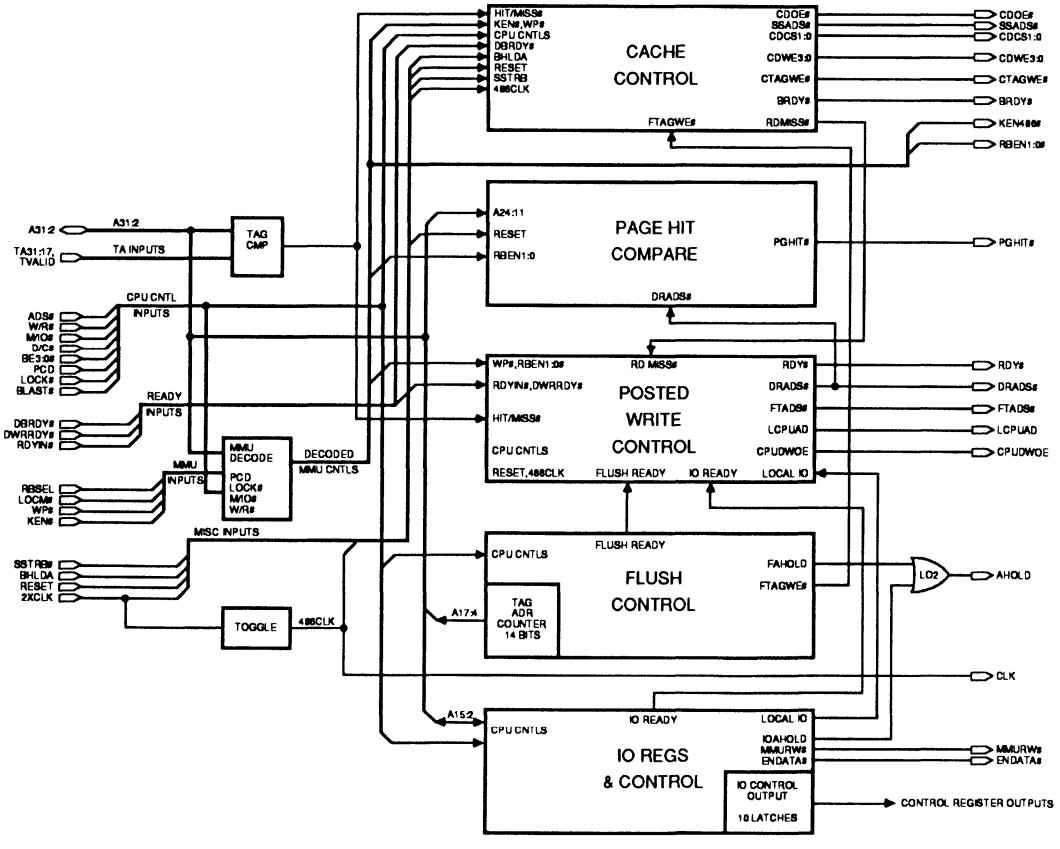


Figure 2: *PLR2KT i486 Cache Control Block Diagram*

Cache Controller Pin-out

Table 1A: CPU Interface Signals

NAME	I/O	DESCRIPTION
A31:18	I	Address lines from the 486 used to compare with the tag information from tag RAMs. Also used to qualify the MMU inputs which are only valid in the low 256 Mbytes of memory. These addresses are also used in the creation of the PGHIT signal for the DRAM controller
A17:2/D7:0 I/O	I/O	These addresses are used to create the PGHIT signal and to select on-chip IO locations. During IO to internal registers AHOLD will be asserted and these pins will be data pins to/from the chip. An external LS245 will be used to route this data from A9:2 to D7:0 and will be controlled with the ENDATA# signal. These addresses will also be output during a flush command for the 486. During this time AHOLD will be active and these lines will count up from 0 to 16K. A CTAGWE# will be issued for each address and TVALID bit will be written low invalidating all tag locations.
BLAST#	I	Burst Last from the 486.
ADS#	I	Address Strobe from the 486.
M/IO#	I	Memory not IO from the 486.
W/R#	I	Write not Read from the 486.
D/C#	I	Data not Code from the 486.
BE3:0#	I	Byte Enables from the 486. Used to select the correct CDWE3:0 line during write operations.
PCD	I	Page Cache Disable from the 486.
LOCK#	I	Indicates a Lock cycle from the 486. A lock cycle is not cached.
CLK	I/O	Clock output to the 486.
KEN486#	O	Cache Enable to the 486. Indicates the current location is cachable.
RDY#	O	Ready to the 486.
BRDY#	O	Burst Ready to the 486.
SSADS#	O	Snoop Strobe ADS. This should be connected to the 486 EADS# input.
AHOLD	O	Address Hold to the 486. Used to gain control of the 486 address bus.

***Table 1B)** Cache Control Signals*

NAME	I/O	DESCRIPTION
TA31:17	I	Inputs from the tag RAMs. TA17 is ignored if a 256K byte cache is implemented. For a 128K byte cache A17 should not be connected to the tag RAMs.
TVALID	I	Tag Valid bit from the tag RAMs. This indicates whether the cache location is valid. Locations are invalidated during flushes and when a SSTRB# occurs during DMA or master cycles.
CDCS1:0#	O	Cache data RAM chip selects for 128K or 256K byte cache. The chip select line is also used by the IDT 71589 CacheRAMs to keep the internal burst address counter from counting when doing a burst read miss that writes into the cache.
CDOE#	O	Cache Data Output Enable.
CDWE3:0#	O	Cache Data Write Enable for each byte.
CTAGWE#	O	Cache Tag Write Enable.

***Table 1C)** DRAM Control Signals*

NAME	I/O	DESCRIPTION
DBRDY#	I	DRAM Burst Ready. This signal from the DRAM controller indicates that the DRAM controller has read information ready to burst to the CPU and cache.
DWRRDY#	I	DRAM Write Ready. This signal indicates that the DRAM controller has completed its write operation.
DRADS#	O	DRAM ADS. Address Strobe for the DRAM controller.
PGHIT#	O	This indicates to the DRAM controller that the current access is within a DRAM page from the last access.
RBEN1:0#	O	RAM Bank Enable 1, 0. These signals indicate to the DRAM controller that bank 1 or 0 is currently being selected.

***Table 1D)** Buffer Control Signals*

NAME	I/O	DESCRIPTION
SSTRB#	I	Snoop Strobe input used to invalidate the external cache and 486 cache locations on DMA or bus master writes.
RDYIN#	I	Ready Indication from the EISA, MCA, or AT buss chip set.
BHLDA	I	HDLA given from the EISA, MCA, or AT chip set. This signal must not be granted until after the CPUDWOE is inactive to insure that the last posted write is complete.
RESET	I	System Reset.
LCPUAD	O	Latch CPU Address and Data. This is used for the single level of posted write and for the DRAM page mode write pipeline.
CPUDWOE	O	Enable the CPU data outputs for writing.
FTADS#	O	Feed Thru ADS. This is the ADS# for the EISA, MCA, or AT chip set. This is issued for all non-DRAM memory cycles and IO cycles which are not contained on chip.

Table 1E) Memory Management Signals

NAME	I/O	DESCRIPTION
RBSEL	I	RAM Bank Select. This signal indicates which bank of DRAM the current address is stored in if LOCM# is active.
LOCM#	I	Local Memory. This signal indicates the current address is in one of the DRAM banks.
WP#	I	Write Protect. This signal indicates the address is in a write protected region.
KEN#	I	Cache Enable. This signal indicates that the current address is cachable.

Table 1F) Miscellaneous Signals

NAME	I/O	DESCRIPTION
2XCLK	I	Two times Clock. This is twice the operating frequency of the 486 and is used to create the 486's clock and the internal clock used on the array.
ENDATA#	O	Enables D7:0 onto A9:2 for IO writes to the on board registers and A9:2 onto D7:0 for IO reads from on board registers.
MMURW#	O	MMU Read or Write operation. Indicates a read or write operation to the MMU. AHOLD will be generated for these cycles.

Table 1G) Signal Pin Summary

Total number of Output pins	22
Total number of Input/Output pins	17
Total number of Input pins	52
Total number of signal pins	91

Table 2: Gate Estimate for the PLR2KT Gate Array

18	D Flip-flop's with 4-Input OR (LFP5)	for Outputs
6	" "	for Posted Write Control
4	" "	for Cache Controls
28	D Flip-flop's with 4-Input OR (LFP5) Total Assume 2 Low Power 4-Input NOR's (LN4U) for each LFP5	
56	Low Power 4-Input NOR's (LN4U) Total Assume 2 Low Power 9-Input NOR's (LN9U) for each LFP5	
56	Low Power 9-Input NOR's (LN9U) Total Assume 2 Buffered 2-Input NOR's (LN2) for each LFP5	
56	Buffered 2-Input NOR's (LN2) Total	
10	Transparent D-Latches (LLP1) for Control Latches	
28	Transparent D-Latches (LLP1) for DRAM Page Latches	
28	Low Power 2-Input Exclusive OR's (LX2U) for DRAM Page Compare	
4	Low Power 9-Input NOR's (LN9U) for DRAM Page Compare	
1	Buffered 2-Input NOR (LN2) for DRAM Page Compare	
14	D Flip-flop's (LFP1) for Tag Flush Counter	
15	Low Power 2-Input Exclusive OR's (LX2U) for Tag Compare	
3	Low Power 9-Input NOR's (LN9U) for Tag Compare	
2	Low Power 2-Input NOR's (LN2U) for Tag Compare	

28	LFP5's	@	14	cells/each	392 cells
56	LN4U's	@	2	cells/each	112 cells
56	LN2's	@	4	cells/each	224 cells
14	LFP1's	@	12	cells/each	168 cells
38	LLP1's	@	8	cells/each	304 cells
43	LX2U's	@	4	cells/each	172 cells
63	LN9U's	@	8	cells/each	504 cells
2	LN2U's	@	1	cells/each	2 cells
					1878 cells
	Add 20% for miscellaneous gates				376 cells
	Total				**2254 cells**

Timing Requirements

1) Cache Timing

The following assumptions have been made for the 50 MHz i486:

CLK to ADR, ADS#, M/IO#, W/R#, D/C#D31:0, DP3:0	11 ns
RDY, BRDY setup time	3 ns
D31:0, DP3:0 setup time	3 ns

It is also assumed that since the i486 CLK and all outputs are generated on the PLR2KT, the clocked outputs will occur nearly simultaneously with the i486 CLK.

Figure 3 shows the basic zero-wait cache write hit timing. To achieve this timing at 50 MHz the following tag RAM timing is required:

Tag Access = (2 CLKs) -
(i486 ADR delay) -
(PLR2KT delay to CDWE3:0#) -
(IDT 71589 WE to CLK)
= 40 ns - 11 ns -
8 ns - 3 ns
= 18 ns

18 ns is well within the 15 ns access time of the CY7C161-15 RAMs which are used for the tag directory.

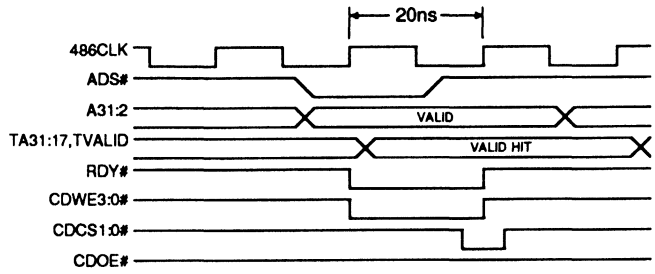


***Figure 3:** Zero Wait Cache Write Hit*

Figure 4a shows the cache tag RAM access required for a zero-wait read hit access. The timing required for this is:

Tag Access = (2 CLKs) - (i486 ADR delay) - (i486 BRDY# setup time) - (PLR2KT delay to BRDY#)
= 40 ns - 11 ns - 3 ns - 8 ns
= 18 ns

18 ns is also within the 15 ns access time of the tag directory RAMs.

Figure 4b is a gate level schematic which shows the path from the TA31:17 and TVALID through the PLR2KT to the BRDY# signal. The worst case delay through this path is 7.9 ns. This number is rounded up to 8 ns and used in the above calculations.

A cache controller design could be done with PLDs and special cache tag RAMs which have the tag compare on the RAM chip. These special RAMs would have to be used because of the pin constraints of PLD devices and because only a single level of PLD delay can be tolerated to return BRDY# or CDWE3:0# signals. These special cache tag RAMs, however, are not currently available in access times below 30 ns at 64K bit sizes. As seen by the calculation below, this is not fast enough to support the zero-wait read hit timing.

Tag Compare Access = (2 CLKs) - (i486 ADR delay) - (i486 BRDY# setup) - (PLD delay to BRDY#)
= 40 ns - 11 ns - 3 ns - 7 ns
= 19 ns (< 30 ns)

In our proposed cache architecture, the IDT 71589 CacheRAM is required to provide a zero-wait write hit to cache. This is because conventional RAMs which don't have a self-timed write require a write pulse before the end of the write cycle to write the data. Figure 5 shows the timing of a zero-wait write hit using conventional data RAMs. The smallest write pulse for devices available today is 8 ns. Given this the TAG access time required would be:

Tag Access = (2 CLKs) - (i486 ADR delay) - (PLR2KT delay to CDWE#) - (CDWDE# pulse width)
= 40 ns - 11 ns - 8 ns - 8 ns
= 13 ns

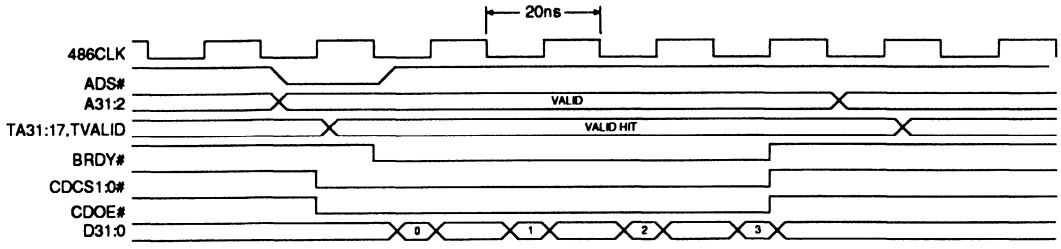


***Figure 4a:** Zero Wait Read Hit*

Figure 4b: *Cache Controller Critical Path*

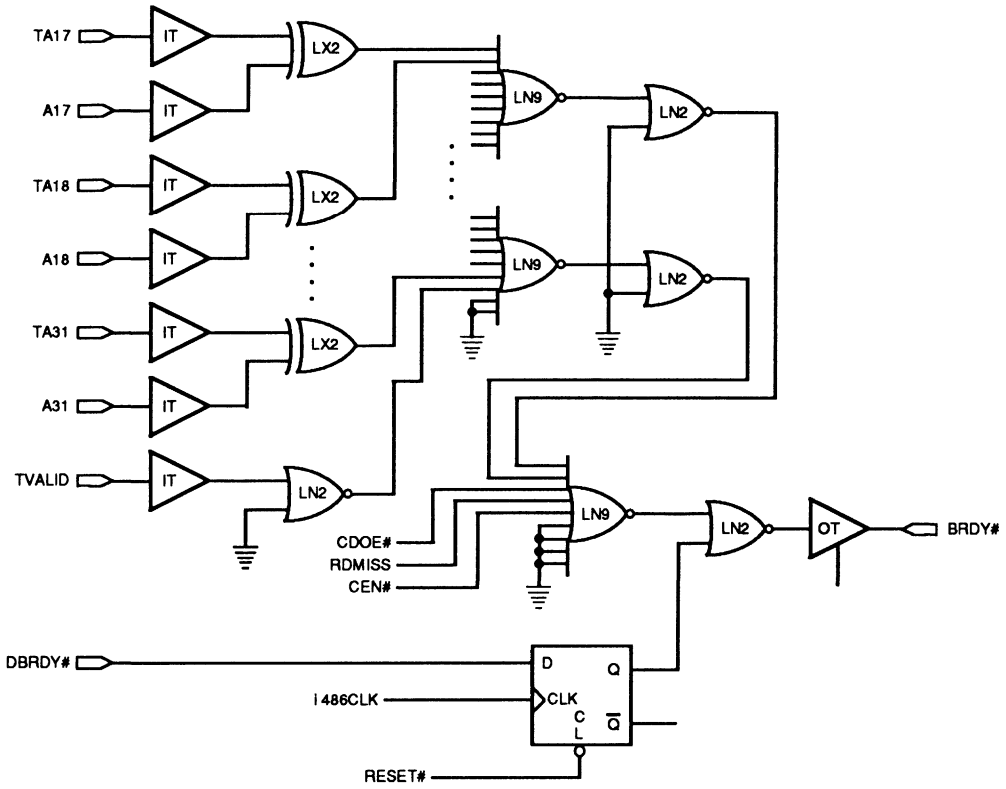
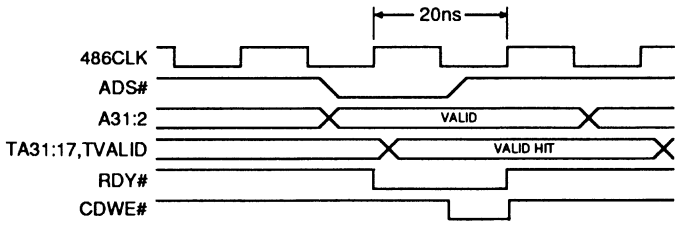


Figure 5: *Zero Wait Cache Write Hit Using Conventional SRAMs*



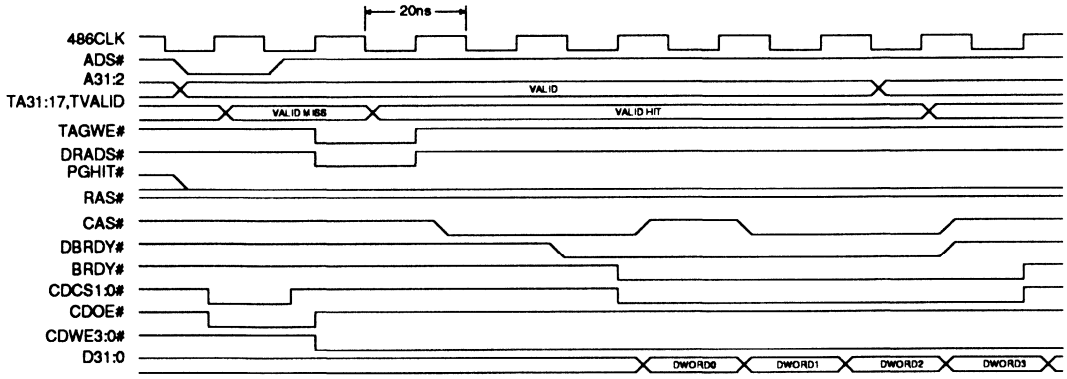


Figure 6: *Cache Read Miss Cycle*

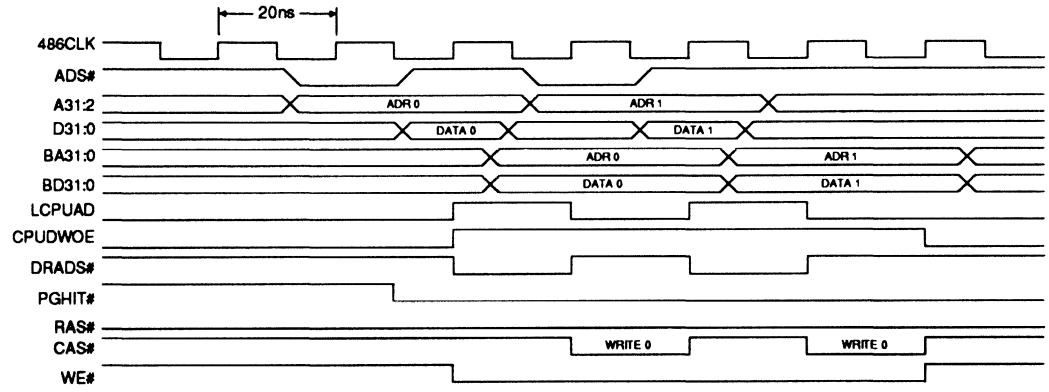


Figure 7: *DRAM Page Hit Write Timing*

It would be very difficult to provide only an 8 ns write pulse width. A 10 ns pulse width would be more likely because it is one 2XCLK period. Because of clock skews and setup time requirements, this would reduce the tag access requirement to 9 ns. When 9 ns 16K X 4 RAMs become available, the need for self timed RAMs for cache implementation will be obviated. Figure 6 shows a cache read miss cycle to DRAM. This results in a burst write into the cache data RAMs.

2) DRAM Timing

Figure 7 shows posted DRAM page hit write timing with zero-wait states. Notice that the bandwidth for write hits is equal to the fastest write timing to the cache. Because of this there is virtually no advantage to implementing a write-back cache. A zero-wait posted write pipeline to DRAM is possible because the CAS write pulse width required for fast page mode DRAMs is only 20 ns.

Also shown in Figure 6 is a burst mode read to DRAM with a DRAM page hit. Notice that after the first Dword is read the remainder of the Dwords can be read at one Dword per clock; the fastest rate supported by the i486. This can only be achieved by using a 64 bit wide (or wider) DRAM array as shown.

DRAM page miss reads and writes will, of course, be slower. The DRAM page size however is quite large since the array is 64 bits wide.

DRAM Chip Size	*Page Size*
256 Kbits	4 Kbytes
1 Megabit	8 Kbytes
4 Megabits	16 Kbytes

3) MMU Timing

The MMU timing needs to be the same as the tag RAM timing to support the write protect feature to the internal and external caches. This is because the write protect signal must be known to decide whether to give the data RAM CDCS1:0# signals on a write hit and to give a EADS# to the i486 by the end of the write to invalidate the location inside the i486.

4) Advantages of the PLR2KT

The PLR2KT has many advantages over PLD based designs. Because of its high speed and large number of pins, all of the time critical functions can be implemented on a single PLR2KT chip. This allows the outputs to have very little skew to the processor clock because all signals are generated on the same chip. Also, because of the limited pin out of the PLD devices, multiple, serial delays may be required which are not necessary on the PLR2KT.

A cache controller implemented with a PLR2KT means that slower tag, data, and MMU RAMs are required for a given CPU speed or that higher CPU speeds can be supported.

The PLR2KT also provides higher integration and lower power consumption than a bipolar PLD implementation. This can translate to smaller boards or more functions per board. It also provides higher reliability, testability, and easier manufacturing than a PLD based design. The PLR2KT also provides benefits over full custom or single chip standard product cache controller approaches. These include: faster time to market, proprietary and/or customer controlled design, higher speeds, and smaller tag block sizes.

The small tag block size improvement is of particular importance. It is due to the fact that, in order to achieve required speeds, custom cache controllers implement the tag RAM in the chip itself. This limits the tag directory size to about 32K bits. With this small tag RAM size, large blocks of cache must be tagged when a large (256Kbyte or bigger) cache memory is used. Block sizes of 64 to 128 bytes will be required to support caches of 256 Kbytes. Block sizes this large will be detrimental to performance in both write-thru and write-back caches. The problem will be particularly critical in a write-back cache because on a "dirty" read or write miss the whole block must be written back to DRAM. This takes a lot of time and buss bandwidth.

By using off-chip SRAM for the tag directory, the PLR2KT implementation of a cache controller eliminates this problem. The tag directory can be fairly large resulting in small, manageable block sizes. Only a GaAs device, such as the PLR2KT, has the internal speed needed to use off-chip RAM and still keep up with 50 MHz processors.

Power Dissipation: BiCMOS vs GaAs

Application Note 10

Introduction

CMOS and BiCMOS have traditionally been viewed as low power technologies. This reputation stems from the fact that unlike other technologies which have preceded them (TTL, ECL, NMOS, etc.) the power dissipated by a CMOS or a BiCMOS gate is dependent on the frequency of its operation. When CMOS or BiCMOS gates are not toggling they dissipate almost no power. As operational frequencies in the gates increase, however, the amount of power dissipated proportionately increases. At these higher frequencies, GaAs Direct Coupled FET Logic (DCFL), which is capable of faster gate delays, dissipates less power than BiCMOS.

The purpose of this application note is to show how both BiCMOS and DCFL GaAs power dissipation is calculated and to examine and compare the two technologies with regard to power dissipation.

Power Calculations for BiCMOS

There is little or no static power dissipated in most practical topologies of BiCMOS gates since current is used exclusively to charge and discharge load capacitance. BiCMOS ASIC design manuals instruct the user to compute the internal cell power dissipation by multiplying a factor, whose units are microwatts/(gate-MHz), by the frequency of operation. This result is then multiplied by the total number of cells in a given design derated by an arbitrary fraction representing the number of gates switching. This latter derating factor ranges from 0.2 to 0.4 depending on the design at hand. The composite power is calculated using the following formula:

$$P_{internal} = F A_V G P_{gm} \qquad (1)$$

Where:

- F = the highest frequency in MHz for gates in the design
- A_V = average fraction of the gates which are switching at a given time
- G = the total number of gates in the design
- P_{gm} = the power per gate-MHz (typically between 20 and 40 microwatts/gate-MHz)

To obtain accurate results from a particular design, however, it would be a mistake to use the A_V estimation factor blindly. Not using any derating factor could also result in an incorrect estimate of the power dissipated in a sequential circuit. Between two successive registers in a sequential circuit there may be several levels of logic. As a result, the effective frequency seen by any one gate in the chain of gates between registers can be substantially lower than the clock frequency applied to the registers. For small designs it is practical to explicitly calculate the effective frequency of operation

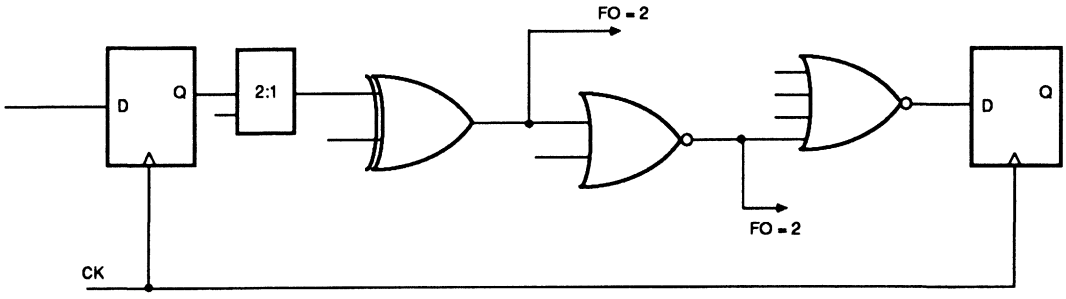


Figure 1: *Benchmark Circuit; This circuit is analyzed in the text to compare its power dissipation vs. frequency when implemented in BiCMOS and GaAs.*

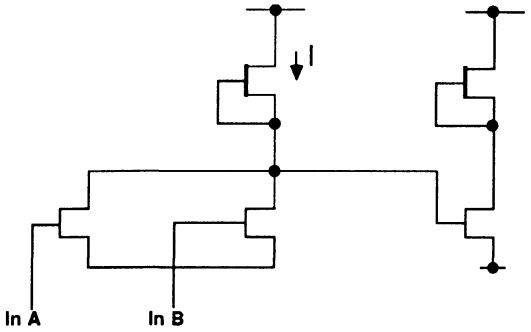


Figure 2: DCFL Logic

of each gate and obtain an accurate understanding of power dissipation.

As an example please refer to the benchmark circuit of figure 1. Here several stages of logic are placed between two flip-flops. The maximum frequency seen by any gate other then the flip-flops is one half of the flip-flop frequency. This is due to the fact that the output of a flip-flop can only toggle at one-half its clock frequency. In addition, there is a statistical probability of 0.5 that the output of a given gate or flip-flop will remain at its previous logic state (assuming an equal number of ones and zeros in the incoming data stream) in which case no power is dissipated since a transition did not occur.

We can split the problem into two; the power dissipated in the flip-flops and the power dissipated in the gates. For the flip-flops the power can be estimated by:

$$Power = F(0.5)GP_{gm} \quad (2)$$

and for the gates in between:

$$Power = F(0.5)(0.5)GP_{gm} \quad (3)$$

Power Calculation for DCFL GaAs Circuits

Unlike CMOS or BiCMOS, DCFL GaAs circuits have a power dissipation which is independent of logic state or frequency of operation. The reason for this can be seen by examining figure 2 which depicts a typical DCFL NOR gate driving an inverter. The DCFL structure is composed of a pull up depletion FET and one or more pull down enhancement FETs. The NOR operation is possible because when both pull down FETs are off (corresponding to a logic low at each input) the logic gate's output voltage rises to a valid logic high. However, when one or more pull down FETs are on (corresponding to a logic high at their input) the pull down FET sinks all of the pull up FET current while maintaining a very small Vds. As a result a valid logic low is created at the gate's output.

GaAs FETs, unlike silicon MOS devices, do not have an insulator between the gate and channel region. Instead they employ the depletion region of a schottky barrier junction to modulate drain to source current. This schottky diode will conduct current between the gate and source when forward biased. In normal DCFL operation, a valid logic high voltage is determined by the forward biased voltage of the gate to source diode. As a result the load current, I, of a DCFL gate will be used to forward bias the gate to source diode of a subsequent logic gate.

In normal operation the current consumption of a DCFL logic gate is constant. Current is simply steered either into the pull down FET in a logic low condition or into the gate to source diode of a subsequent logic gate in a logic high condition. For high speed logic this situation is ideal because current, and subsequent voltage, "spiking" on power supply lines is eliminated.

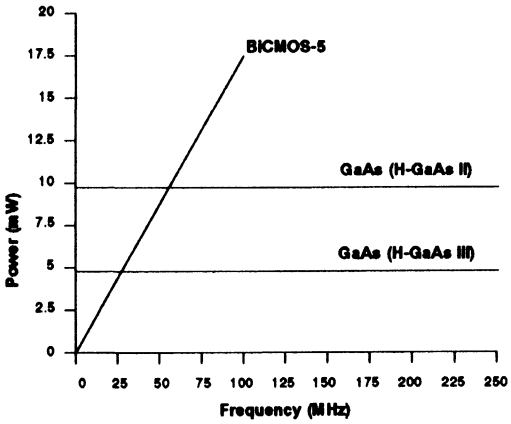
Therefore, when calculating the power dissipation of a DCFL based chip, the power dissipation reported for an individual logic macro is valid for any frequency at which it can operate.

Benchmark Circuit

To get an idea of the range of speeds and power dissipations achievable in both BiCMOS and GaAs technology we turn our attention again to the benchmark circuit of figure 2. Table I shows the delay for each macro in both BiCMOS and GaAs technology. For the BiCMOS portion of this analysis the NEC BiCMOS-5 design manual was used. The Vitesse FURY manual was used for the GaAs

MACRO	DELAY (BICMOS)		DELAY (GaAs)	
	Rising	Falling	Rising	Falling
F/F CLK→ Q	2.75	2.59	0.59	0.36
2:1 MUX (Fo = 1)	1.93	2.10	0.61	0.28
2 Input XOR (Fo = 3)	1.66	2.10	1.34	0.45
2 Input NOR (Fo = 3)	1.26	0.50	1.15	0.56
4 Input NOR (Fo = 1)	2.66	0.45	0.49	0.26
F/F Setup Time	0.25	0.25	0.14	0.14
Rising Delay	9.97 nS		3.73 nS	
Falling Delay	9.96 nS		3.20 nS	
Max Operating Freq.	100.2MHz		268.1 MHz	

Table I: *Macro Delay*



Source: NEC BICMOS-5 Design Manual, Oct. '89
Vitesse FURY Design Manual, v. 3.0

Figure 3: *Power Dissipation vs. Frequency for Benchmark Circuit*

portion.

As seen from Table I the delays for both rising and falling output waveforms were calculated. Because NOR gates cause signal inversion the worst case delay through a network must be calculated by evaluating all realistic propagations through the cascade of gates taking signal inversions into account. The worst case path for each situation is designated by arrows in Table I.

Table I indicates that, for the benchmark circuit, the maximum frequency attainable in BiCMOS is 100.2 MHz. GaAs technology is capable of a 268.1 MHz frequency. The GaAs macros selected for this particular analysis are optimized for low power dissipation. As a result a factor of 2.7 improvement in speed is observed between GaAs and BiCMOS. A greater investment in power could yield speed improvement factors of between 4 and 5.

Table II and the corresponding graph in Figure 3 (see page 4) depict the power dissipated by each technology as a function of frequency for the benchmark circuit. The power for the BiCMOS circuit was calculated using equations (2) and (3). The Pgm value NEC attributes to their BiCMOS-5 process is 0.038 mW/MHz.

As seen in Figure 3, the crossover point between the linear BICMOS power curve and the constant GaAs power curve occurs at about 60 MHz with the H-GaAs II process and at about 30 MHz with the H-GaAs III process. Since, for the circuit in question, BiCMOS is limited in frequency to about 100 MHz one can only speculate about the power it would

BICMOS

FUNCTION	BICMOS-5 MACRO NAME	POWER DISSIPATION (mW)			
		25MHz	50MHz	90MHz	100MHz
Flip-Flop	F641	1.42	2.66	4.56	5.7
2:1 MUX	F571	0.47	0.95	1.52	1.9
2-Input XOR	F511	0.47	0.95	1.52	1.9
2-Input NOR	F202	0.24	0.475	0.76	0.95
4-Input NOR	F204	0.24	0.475	0.76	0.95
Flip-Flop	F641	1.42	2.66	4.56	5.1
		4.26	8.55	13.69	17.1

GaAs

FUNCTION	FURY MACRO NAME	POWER (mW)	
		H-GaAs II	H-GaAs III
Flip-Flop	LFPIU	3.1	1.55
2:1 MUX	LMIU	1.3	0.65
2-Input XOR	LXIU	1.7	0.85
2-Input NOR	LN2U	0.33	0.16
4-Input NOR	LN4U	0.33	0.16
Flip-Flop	LFPIU	3.1	1.55
		9.86	4.92

Table II: *Macro Power*

dissipate if capable of higher frequencies. However, since the curve is linearly increasing it is safe to say that at frequencies above 150 MHz BiCMOS power dissipation is unreasonably high.

Conclusion

BiCMOS, which has earned a reputation as a low power technology, earns that reputation at low frequencies only. Since its power dissipation increases linearly with frequency, GaAs technology actually dissipates less power at frequencies above 60-70 MHz. This capability coupled with the fact that GaAs technology is capable of speeds which range between a factor of 3 to 5 faster than BiCMOS positions GaAs as the dominant technology for any high speed digital application.

The Effects of Simultaneously Switching Outputs in GaAs ASIC Devices

Application Note 11

Introduction

When one or more outputs of a semiconductor device switch, a change in voltage is effected on the driven signal lines. This change in voltage is in turn received by any inputs connected to those signal lines and interpreted as a change in logic state. Switching a group of outputs simultaneously, however, may cause undesirable effects on the operation of a circuit. These unwanted consequences are generally referred to as simultaneously switching output (SSO) effects. Features have been incorporated into the design of all Vitesse devices (die and packages) which minimize the deleterious effects of SSO's. These effects have been characterized by Vitesse using a test chip personalization of the FURY VSC10K gate array packaged in a multilayer ceramic 211 pin grid array.

The purpose of this application note, therefore, is to help the system designer minimize the probability of device or board level problems associated with SSO's. This will be accomplished by presenting the designer with some of the physics associated with output switching phenomena as well as some of the methods used to alleviate the effects of SSO's.

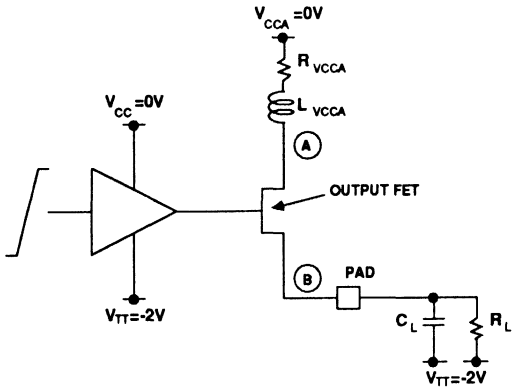


Figure 1: *ECL SSO Model*

Statement of Problem

Simultaneously switching outputs can cause the following effects:

- Additional output delay
- Ground or power supply noise at the device
- Ground or power supply noise in the system
- Noise on adjacent signal pins which share supply or ground pins

Electrical Effects of Output Switching: a Basic Model

Figure 1 shows an ECL source-follower output driving a capacitive load and a 50Ω resistor. Figure 2 demonstrates the relationship between the drain voltage of the output FET (node A) and the source voltage of the output FET (node B) as a pulse is propagated through the ECL output. When the output switches from a logic low state to a logic high state, a substantial gate to source voltage is applied to the output FET causing its source-drain conductance to increase dramatically. As the transient current is conducted through the device to charge the capacitive load, an instantaneous demand for current is placed on the VCCA (output ground) supply terminal of the output node A. If inductance is present in the VCCA supply path (as shown in Figure 1), the voltage at node A will drop until the inductor is energized and necessary current can be supplied to the output FET. A falling output edge conversely creates a positive transient voltage on the VCCA node. Increasing the inductance in the tends to impede the transient current flow and increase the size of the SSO noise pulses shown in Figure 2. At the system level, these effects are manifested as degradations in the pin-to-pin delay of a device. In addition, if sufficient noise is coupled from the VCCA pins to the VCC supply in the device, the

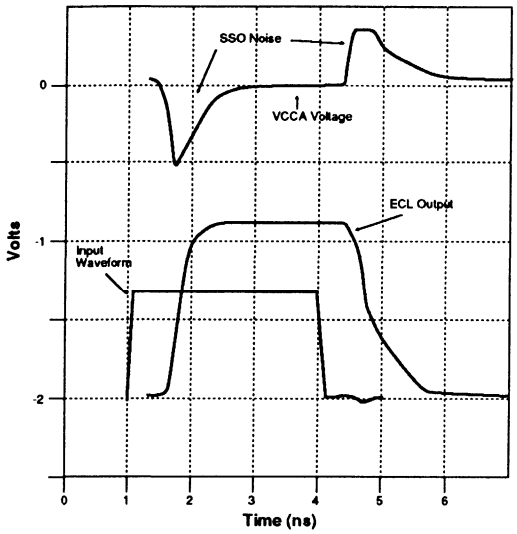


Figure 2: *Power Supply Noise*

states of synchronous elements (registers or latches) in the core of the device may be altered causing the circuit to logically fail.

ASIC Device and Package Features to Alleviate SSO Problems

All of Vitesse's high-performance packages are designed to minimize the electrical problems associated with simultaneously switching outputs. The power and ground pads on each device are fixed. These pads are bonded to separate planes in the multi-layer ceramic package. In order to isolate critical asynchronous inputs (such as clock and reset signals) from noise generated by output switching, outputs on Vitesse devices are confined to the top and bottom of the die (see Figure 4). Signals which are sensitive to noise can then be brought onto the device though input buffers on the left and right sides of the die. This not only isolates the inputs and outputs on the die itself but also minimizes mutual coupling (crosstalk) between output and input bond wires by placing them at 90° with respect to one another.

SSO Test Chip Description

Output Registers

In order to gain an empirical understanding of the effects of switching large groups of outputs on a large device, Vitesse has designed and produced a test chip specifically designed to examine these effects. The schematic of the test chip is shown in Figure 3. The SSO test chip, or SSOTC, is implemented using a Vitesse FURY VSC10K gate array in a 211 PGA package. The test circuitry consists of 80 shift registers grouped into four banks of 20 registers each. Each shift register contains four D flip-flops. The four Bank Scan signals allow data on the SDAT (scan data) bus to be clocked into the shift registers on a bank by bank basis. The input CLOCK serves as the system clock for both scanning and shifting operations. To reset all the registers at once, the RESET signal can be asserted. The BZ bus signals allow the

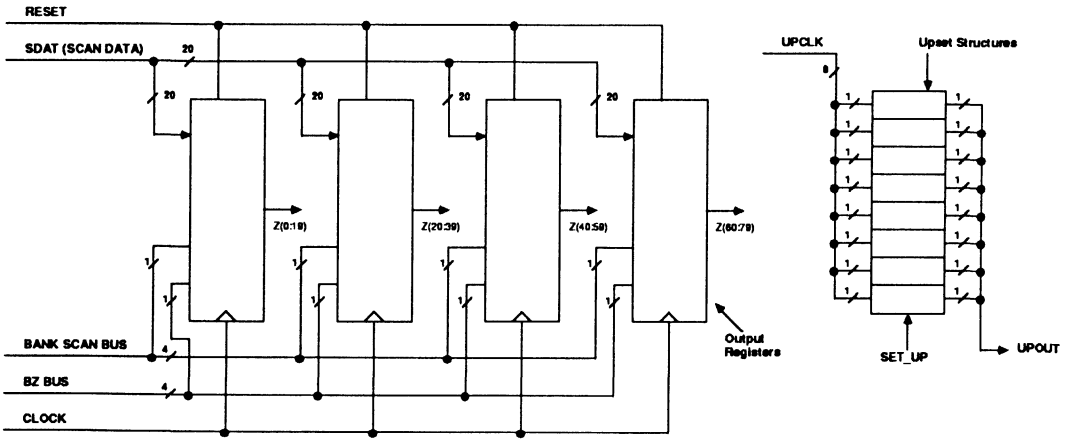


Figure 3: *SSO Test Chip Schematic*

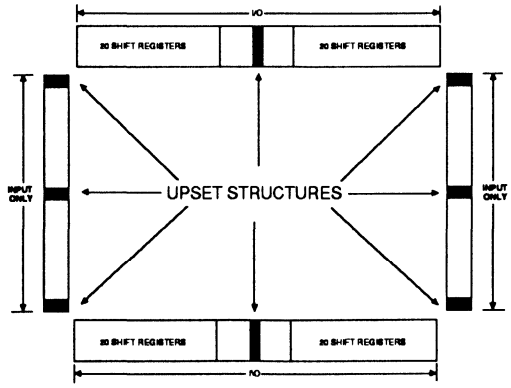


Figure 4: *SSO Test Chip Block Diagram*

user to force the outputs of given bank to logic low without resetting the registers in the bank. Using the scan inputs, patterns which switch anywhere from one up to 80 outputs can be scanned in and clocked to the Z outputs.

As with all FURY gate arrays, the power and ground pins are in fixed locations. In order to minimize the undesirable effects of simultaneous output switching, every four outputs typically share a "dirty" ground, or VCCA, pad. The VCCA pads are in turn bonded to conductor planes in the 211 PGA package. The purpose of the VCCA pins is to decouple switching noise from the internal VCC supply used by the core logic of the device.

Upset Structures

In order to monitor the coupling of noise back into the SSO test chip, eight upset structures are interspersed around the periphery of the gate array as shown in Figure 4. Each upset structure consists of a D flip flop (FURY LFP3 macrocell) configured so that it will toggle on an active clock edge. The clock inputs of these structures (UPCLK bus) are driven by ECL input pins. The outputs of these structures are connected directly to ECL outputs (UPOUT bus). If the noise generated by the simultaneous output switching is sufficiently coupled to the upset structure input, the flip-flop will toggle, thus signifying an upset failure.

SSO Test Results

Characterization of SSO effects was performed on a Teradyne J953 VLSI tester. In order to execute a given test, all the shift registers are first reset and then logic highs are shifted into the registers whose outputs are to switch. The master clock is then used to shift the pattern to the outputs causing first a group of simultaneous rising edges and then a group of simultaneous falling edges.

Simultaneous Switching Delay

The effects of concurrent switching on output delay were measured by connecting both the CLK signal and one of the Z outputs, to a high speed oscilloscope while the test chip is in the Teradyne test fixture. The tester was then used to force various switching patterns on the part while the relative delay was monitored. During the initial testing, it was determined that most of the observed SSO delay was due to the device test fixture. The test fixture was reworked to minimize the impedance to the VCCA pins. Subsequent testing showed a minimal delay degradation as increasing numbers of outputs sharing the same VCCA pin were switched. Analysis of the delay data showed the following typical delay per output switched:

$$T_{pd}(SSO) = 15\,ps/SSO$$

for ECL outputs which share a common VCCA pad.

A maximum total delay degradation of approximately 100 ps was observed when switching up to six ECL outputs sharing the same VCCA pad. Increasing the number of

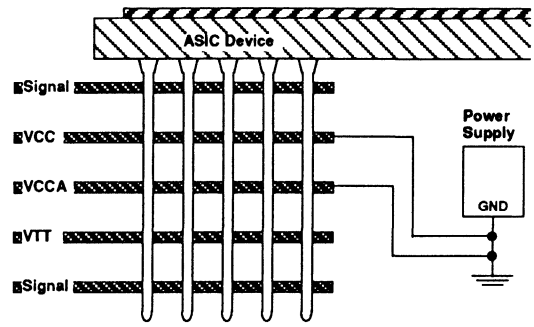


Figure 5: *Recommended Ground Distribution*

outputs switching beyond six, however, appeared to have a negligible effect on the output delay.

Simultaneous Switching Noise

A second phase of testing was performed to characterize the coupling of SSO noise to input pins. For these tests, various combinations of the Z outputs were switched and the states of the upset structure outputs (UPOUT bus) were monitored. No upset structure failures were observed when switching up to 40 outputs simultaneously. Results for more than 40 outputs switching were inconclusive due to the noise inherent in the VLSI test environment. As previously noted, however, SSO noise in the device appeared to be primarily a localized effect. The design of the pad ring on the FURY 10K as well as the design of the 211 PGA itself appears to accommodate the switching of all 100 ECL outputs on the device simultaneously with no effect on internal logic states.

System Design Recommendations for Minimizing SSO Effects

To minimize the possibility of SSO related problems in a given system, precautions should be taken in the arrangement of the inputs and outputs on the ASIC as well as in the construction of the board on which the integrated circuit(s) will reside. The following guidelines summarize these precautions.

ASIC and Board Design Guidelines

1. Place all clock, set, or reset signals on the ASIC at least six pads away from any output.

2. When designing a custom pad ring, a) a VCCA pad should be allotted for each set of four ECL or GaAs outputs, and b) two VCCA pads and a VTTL (+5 V) pad should be allotted for each set of eight TTL outputs.

3. Separate planes should be used on the PC board for VCC and VCCA. (See Figure 5.) These planes should be joined only at the ground terminal of the power supply (the point of lowest impedance).

4. If separate planes on the PC board are not feasible for VCC and VCCA, then a single layer can be used for both. VCC and VCCA, however, should be isolated from one another (confined to separate sections of the board) and connected at the ground terminal of the power supply (Figure 5).

5. The peak switching current should be estimated for the worst case number of SSOs per device and adequate bypass capacitance should be added to satisfy the transient VCCA and VTTL current needs.

Bypass Capacitor Recommendations

Bypass capacitors must be used in high frequency (>100MHz) designs to filter out high frequency variations in the power supply voltages at the device power inputs and on the board. The following bypassing is recommended.

1. A 0.01μF high frequency capacitor should be placed between ground (VCC) and each V_{TT} (-2Volt) pin as close to the V_{TT} pin as possible.

2. A 1 to 10 μF capacitor should be placed on the board at the power supply inputs to filter out variation in the power supply with longer time constants (e.g. power supply noise at the system clock frequency.)

Technology Translation: Converting Silicon Designs to Vitesse ASICs

Application Note 12

Introduction

This application note describes a general method for converting a design implemented in one technology into another technology using the Synopsys Design Compiler™. Specific guidelines are given for converting a "non-GaAs" design (e.g. CMOS, BiCMOS, ECL) into a Vitesse gate array or standard cell implementation. This document also contains specific information on converting PLD equation-based designs into Vitesse ASICs.

Technology Translation Basics

The low speed-power product and high integration level possible with current Vitesse H-GaAs technology has created a need to translate designs from various Silicon-based technologies into Gallium Arsenide Direct-Coupled FET Logic (DCFL). Prior to committing to a redesign, high-performance systems houses need a method to evaluate the performance, power, and size of their existing designs were they to be re-implemented in GaAs. Until recently, such translations could only be accomplished by either manually swapping logic functions from one technology to another on a workstation or by redesigning from the ground up using the alternate vendor's library. Both of these methods involve a great deal of effort and are prone to errors. Logic synthesis tools such as the Design Compiler™ from Synopsys, however, remove most of the manual tasks and result in virtually error-free design conversions.

General Translation Flow

Figure 1 shows the sequence of events and the files involved to translate a design from one technology to another. Two alternate paths are shown - the left path is used if an EDIF netlist is not available. The actual translation is carried out by the Synopsys Design Compiler™ using

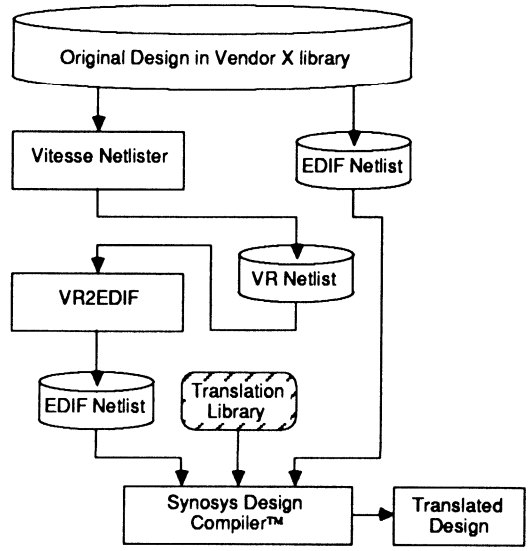


Figure 1: *Design Transition Flow*

the **link** command. Figure 2 shows the libraries needed for translation.

Original Library

This library contains all of the cells which are referenced in the original design. This may be a library from another (non-Vitesse) vendor or may be a Vitesse ASIC library (e.g. FURY gate array). If this library does not exist it can readily be created for the subset of cells which are used in the original design. Refer to the Synopsys Library Compiler Reference Manual for information on creating Synopsys libraries.

Translation Library

This library contains designs (cell descriptions) which are named after the sequential and tri-state elements from the

Figure 2: *Translation Libraries*

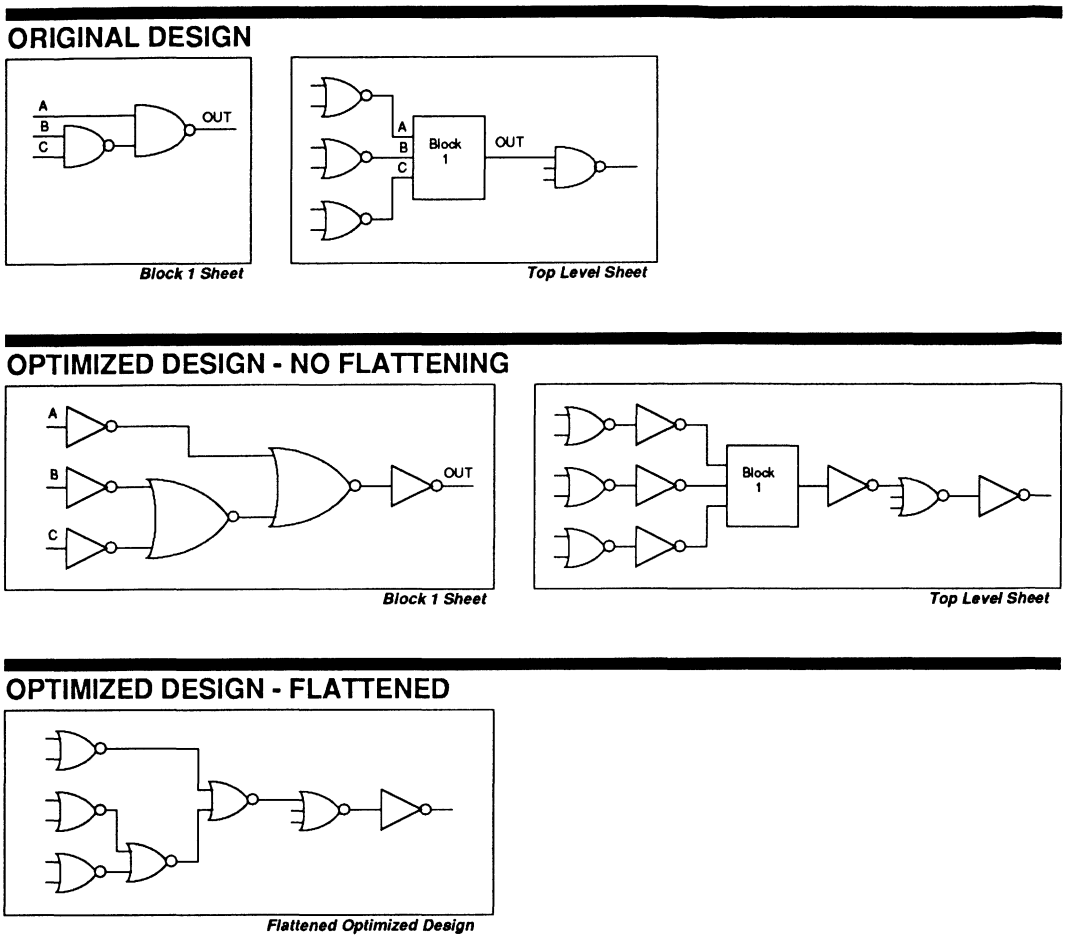


Figure 3: *Optimizing a Hierarchical Design*

original library, but are described using cells from the desired Vitesse library. The user should note that all non-combinatorial functions as well as any tri-state functions in the original library must be mapped into the Vitesse library by creating entries in the translation library. Combinatorial functions such as AND gates, multiplexers, etc. need not be mapped explicitly by the user because the Synopsys Design Compiler™ can automatically (and unambiguously) map such functions between technologies.

Translating Hierarchical Designs

Designs may be converted from another technology into a Vitesse ASIC-based implementation regardless of whether the designs are hierarchical or flat. The conversion methodology used, however, depends upon the user's desire to preserve the original hierarchy present in the design after it has been converted. In making this choice, the following issues should be considered:

- *How large is the design?*
  If the design is in excess of 10,000 gates, the user may wish to convert hierarchical blocks individually and then link them in the Design Compiler™ at the end of the conversion. This not only preserves some of the original hierarchy in the design, but also requires far less computing resource (e.g. RAM and disk space) than converting the entire design at once.

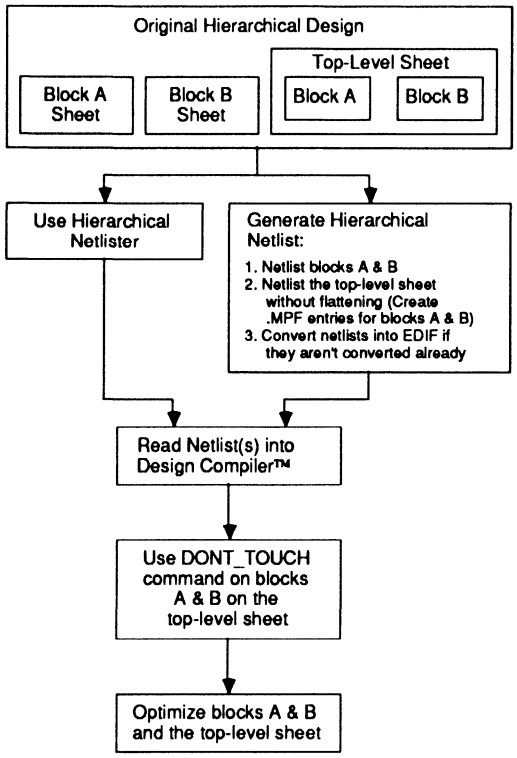


Figure 4 *Hierarchical Conversion Flow*

- *Do optimized designs for some of the blocks already exist?*
  The design may contain, for instance, a 32-bit adder implemented using CMOS NAND-based structures. Several versions of 32-bit adders optimized for Vitesse GaAs DCFL implementations already exist. Thus, the user may choose not to convert this block at all and opt to use an existing block can be provided by Vitesse.

- *Will preserving the hierarchy produce a less than optimal design?*
  In certain designs, the original hierarchy (especially at the lowest levels) may make the application of optimization algorithms such as (DeMorgan equivalent circuits) difficult if not impossible. Figure 3, for example, shows an original hierarchical design and two different optimizations - one without flattening and one with flattening. The optimal design in terms of speed, power, and area is the flattened version. Keeping the hierarchy intact, however, will produce an optimized design similar to the one shown in the center of the figure.

Figure 4 shows the conversion flow for a hierarchical design. Note that some of the steps in this flow are not necessary if the user can provide a hierarchical EDIF netlist to Synopsys.

Conversion Example

Figure 5 shows a 4-bit counter design in Vendor A's technology which is to be implemented as a Vitesse FURY gate array. The following steps are used to translate this design:

1. *Create the translation library.*
   The translation library is generated by creating representations of the sequential elements (D flip-flops, latches, etc.) and tri-state elements (tri-state outputs and internal buffers) in the Vitesse FURY library. In this example, Vendor A's library contains a D flip flop with Q and QN outputs not present in the FURY library. Therefore, the design shown in Figure 6 must be created to represent the

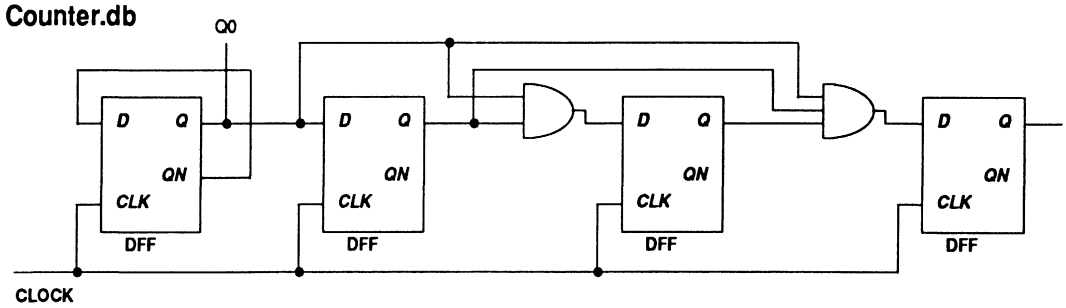


Figure 5: *Four Bit Counter in Vendor A's Technology*

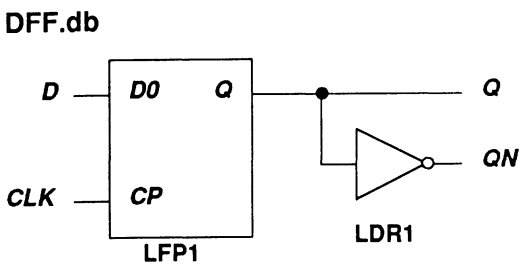


Figure 6: *Vendor A's DFF Macro Mapped into FURY*

Vendor A's flip flop named DFF. In FURY library elements, an LFP1 D flip flop and an LDR1 inverter are combined to create Vendor A's DFF. (Note that the mapping of the LPF1 to the DFF flip flop would be necessary even if the two flip-flops were functionally identical.) The design *must* be named DFF.db and the port names *must* match the port names in Vendor A's cell.

2. *Create the link path.*
   To create the link path, we issue the following statement on the Design Compiler™ command line:

   link_path = {translation_lib.db, vendor_a.db, fury.db}

   This statement assumes that the translation library which contains our newly created DFF.db is named 'translation_lib.db' and Vendor A's Synopsys technology library is named 'vendor_a.db'. The 'fury.db' library will reference Vitesse's FURY library. The **search_path** statement in the **.synopsys** startup file should contain the path or paths where all these libraries are located.

3. *Read in the top level of the original design.*
   In our example, the counter only has one level of hierarchy so we read in the design as follows:

   read counter.db

4. *Translate the design using the* ***link*** *command.*
   The **link** command resolves the references to the non-combinatorial elements using the translation library we have created. These non-boolean elements (such as our DFF) are resolved in exactly the same way the Design Compiler™ resolves any hierarchy.

   link;

   At this point, the design is represented in a mix of Vendor A's technology library (the boolean elements) and the Vitesse FURY technology library (the LFP1 flip flop).

5. *Compile the design to complete the translation.*
   Now we must issue the **compile** command to translate the boolean elements and eliminate the extra level of hierarchy that the **link** command created.

   compile -no_flatten -no_structure -map_effort low;

   Note that the flattening and structuring functions in the Design Compiler™ are turned off and the mapping effort is reduced to its minimum level. This causes the design

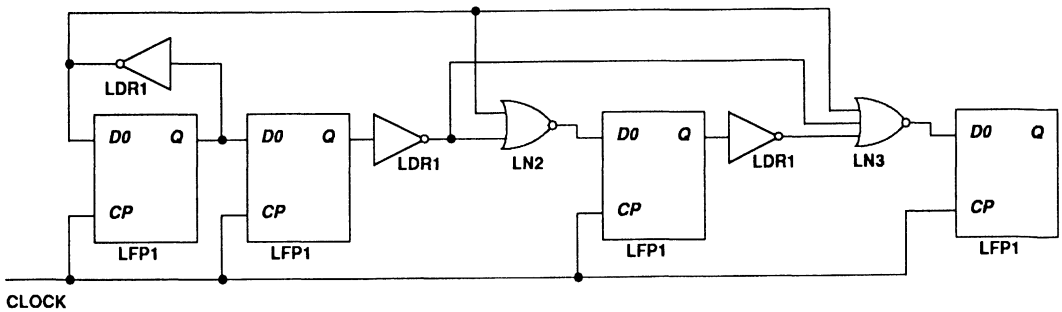


Figure 7: *Four-Bit Counter Translated into FURY*

```
current_design = "TOP";
current_library = "vendorA.db";
translate_library = "vendorA_to_FURY.db";
target_library = "fury.db";
link_path = { translate_library  current_library  target_library };
link;
compile -no_flatten -no_structure -map_effort low;
```

Figure 8: *Example Translation Script*

to be mapped without any logic optimization. Given the CPU time and disk space normally involved with the translation of a large design, this is highly recommended. Figure 7 shows the original design after it has been translated into the FURY gate array library.

6. *Write the translated design.*
   Use the write command to save the translated design in the Synopsys .db format.

   write;

Design Optimization

Merely mapping the design into GaAs DCFL ignores tremendous gains in terms of circuit speed and area which can be realized by using the optimization capabilities of the Synopsys Design Compiler™. The **compile** command allows the user to control the optimization process by designating different optimization routines and amounts of computational resources. Design optimization is also controlled by setting constraint variables (e.g. **max_area**, **max_delay**, etc.) to their desired values. Further details on the design optimization process can be found in the Synopsys Design Compiler™ Reference Manual. Figure 9 shows an example of a script which optimizes a design for minimum area. Area optimization is generally the easiest type of optimization to perform because the desired goal (i.e. zero area!) is the easiest to describe.

```
current_design = "TOP";
link_path = { fury.db };
target_library = { fury.db };
max_area 0.0;
```

Figure 9: *Example Min. Area Optimization Script*

Converting a PLD-based Design into a Vitesse ASIC Design

Vitesse supports the conversion of various PLD descriptions into Vitesse ASIC designs. The conversion is accomplished using the Synopsys Design Compiler™ in conjunction with specific software developed by Vitesse. PLD file conversion is provided as a service by Vitesse and may be a part of a full turnkey development or a "standard" customer design. This section covers the PLD conversion flow and the PLD file types currently supported.

Conversion Flow

Figure 10 shows the general flow for PLD conversion. The customer supplies files for one or more PLD devices to Vitesse. These files are combined and then translated into two files used as input for the Synopsys Design Compiler™:

- Equation File - This file describes the combinatorial logic which feeds the state elements in the design.
- EDIF Frame File - This EDIF schematic file contains a reference to the combinatorial block described by the equation file as well as connectivity information for all the registers, buffers, and I/O cells in the design.

The equation file is read into the Synopsys Design Compiler™ and is compiled and optimized using customer-provided area and speed constraints, if any. The EDIF frame file is then read into the Synopsys Design Compiler™

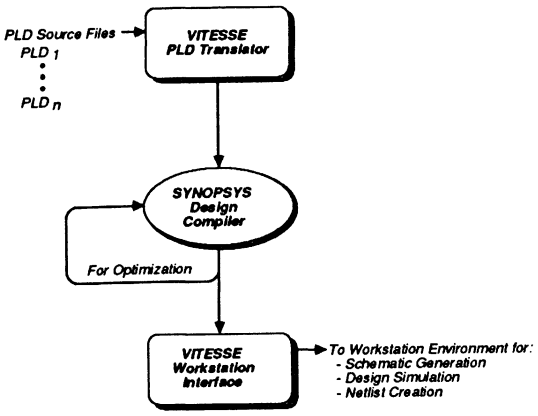


Figure 10: *PLD Conversion Flow*

and mapped into the VITESSE ASIC library. The two descriptions are then linked and the output files are produced in one of two formats depending on the design flow.

Customer Input Files and Design Information Required

This section summarizes the input files and information required by Vitesse to perform a PLD design conversion. The specific file formats indicate those currently supported by Vitesse. PLD conversion support is constantly being reviewed and upgraded, and the user is urged to contact Vitesse if the conversion of file types other than those listed is desired. All of the file informationshould be supplied on one of the following computer media:

Computer Media Supported

- IBM PC, XT, or AT 5.25" floppy disk - any density
- Apple Macintosh 3.5" floppy disk - any density
- SUN cartridge tape
- Mentor cartridge tape

PLD Design Input

1. ***PLD file(s)*** - The customer must supply Vitesse with one or more files which describe the functionality of the PLDs to be converted. These must be on one of the types of computer media named above. Vitesse currently supports the following input file formats for PLD conversion:

- ABL DOC - Equations should be in the format produced by the document module of the ABL compiler. All comments and other extraneous data such as line feeds, form feeds, etc. should be stripped from this file. The file should only contain equations. The following is an example of an equation in ABL DOC file format.

  SIGOUT1 := IN1 & !IN2 & C0 &
  !STOP & GO &
  # MAYBE & BARNEY & WILMA &
  DINO & !BAMBAM
  # BEDROCK & !SIGOUT;

  The := signifies that SIGOUT1 is a registered output. An equal sign with no colon denotes a purely combinatorial output. The ampersand (&) is a logical AND, the pound sign (#) is a logical OR, an exclamation point (!) represents an inversion, and a semicolon (;) ends the equation. No line continuation character is required.

- CUPL DOC - The stipulations listed for ABL DOC files also apply here. The file should only contain CUPL "DOC" format equations. The following is an example of an equation in the CUPL DOC format.

  OUT1.d => !IN1 & IN2 &
  CYCLE1 & CYCLE2 & CYCLE3
  # OLD_DOG & POOCH &
  !MUTT & !OUT1 & PUP

  As in the ABL DOC format, the ampersand represents a logical AND while the pound sign signifies a logical OR. Unlike the ABL format, however, a '.d' suffix is used to denote a registered output. The assignment operator is an equal sign followed by the greater than symbol (=>). There is no semicolon at the end of an equation.

  Vitesse prefers that the customer supply the PLD description as one file.

```
*******************************************************************************
                                    COUNTER
*******************************************************************************

CUPL        3.00 Serial# 999999999
Device      p20r6   Library DLIB-h-24-10
Created     Wed May 16  15:32:49  1990
Name        COUNTER
Partno      none
Revision    1
Date        4/23/90
Designer    George Jetson
Company     Spacely Sprockets
Assembly    none
Location U1

-------------------------------------------------------------------------------
                          Expanded Product Terms
-------------------------------------------------------------------------------

Q1.d =>
    !Q1
Q2.d =>
    Q1
Q3.d =>
    Q1  &  Q2
Q4.d =>
    Q1  &  Q2  &  Q3

-------------------------------------------------------------------------------
                              Symbol Table
-------------------------------------------------------------------------------

Pin Variable                                  Pterms Max    Min
Pol Name            Ext    Pin    Type        Used   Pterms Level
--- --------        ---    ---    ----        ----   ----- -----

    Q1                     21     V           -      -     -
    Q1              D      21     X           1      1     1
    Q2                     20     V           -      -     -
    Q2              D      20     X           1      1     1
    Q3                     19     V           -      -     -
    Q3              D      19     X           1      1     1
    Q4                     18     V           -      -     -
    Q4              D      18     X           1      1     1
    CLK                    1      V           -      -     -

LEGEND:   F : field          D : default variable       M : extended node
          N : node           I : intermediate variable  T : function
          V : variable       X : extended variable      U : undefined
```

Figure 11: *CUPL DOC File for a 4-bit Counter*

For instance, if the customer wants to implement a state machine, the preferred PLD input format is a single equation file which describes the combinatorial logic feeding the state elements as if it were written for one large PAL. If multiple equation files are supplied to Vitesse, all of the names must be unique unless the user want those signals shorted together.

2. ***I/O Designation*** - The customer must also provide a file which lists all of the primary inputs, outputs, and bidirectionals in the "target" design. The following is an example of the I/O designation file:

   I/O Designation File Format
   .inputlist
   IN1
   IN2
   DATA1
   DATA2
   .outputlist
   OUT1
   OUT2
   OUT3
   Q0
   Q1
   Q2
   .bidirlist
   BID1
   BID2

3. ***PLD Connectivity File*** - If multiple sets of equations are provided to Vitesse, the customer must also supply a netlist which describes the connectivity of the PLDs in question. The preferred formats are EDIF or VR (Vitesse internal format). Most workstations provide EDIF netlisting capabilities. Otherwise, if the board design containing the PLDs has been captured on the Mentor or VALID, then a VR netlist can be obtained by running the Vitesse netlister. The customer should also provide a hard-copy schematic which shows the connectivity visually.

PLD Conversion Example

Figure 11 shows an example CUPL DOC file for a 4-bit up counter. The pld2synopsys translator is used to convert this file into the two files (equation file and EDIF file) needed by the Design Compiler™ for conversion of the PLD. The usage of the command is:

pld2synopsys
[-cupl | -abl]
[-pad] [-oe] input_file

where:

-cupl | -abl denotes the input file format: -cupl for a CUPL DOC file and -abl for an ABL DOC file.

-pad causes the translator to add input and output buffers to the design. The -pad switch should be omitted if several PLDs are incorporated in a single conversion.

-oe causes any output enable signals to appear as outputs to the PLD core if the -pad switch is not chosen. If the -pad switch is chosen, then the output enable signals are connected to the output

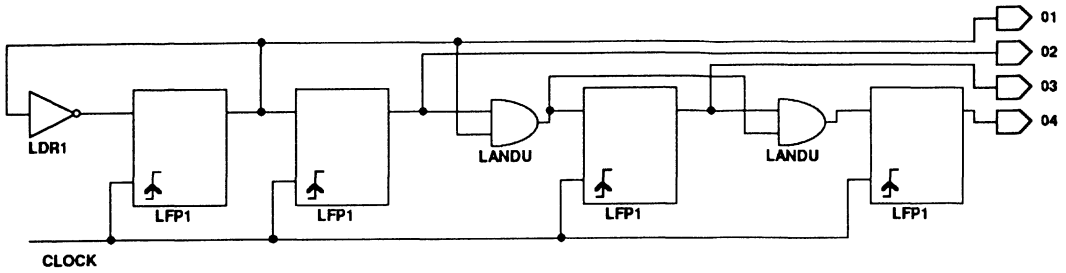


Figure 12: *4-bit Counter in FURY Synthesized from CUPL Equations*

enable inputs of the tri-state outputs.
input_file is the ABL or CUPL input file name

The following command was used to translate the PLD equations in the example into an EDIF and equation file for subsequent reading into the Design Compiler™:

pld2synopsys -cupl counter.doc

Figure 12 shows a plot of the converted design produced by the Design Compiler™. Note that in this case, the design was synthesized for minimum area as opposed to the design shown in Figure 7 which is optimized for speed.

Summary

Vitesse can supply both the guidelines and software necessary for converting a design from a Silicon (Bipolar ECL, CMOS, or BiCMOS) implementation into a GaAs DCFL implementation. The conversion may be performed at the customer location or in-house by Vitesse. For more detailed information on the capabilites of the Synopsys Design Compiler™, the following sources are recommended:

Synopsys™ Design Compiler™ Reference Manual. Synopsys, Inc. Version 1.2, October 30, 1989.

Synopsys™ Design Compiler™ Commands Reference. Synopsys, Inc. Version 1.2, November 30, 1989.

Synopsys Technical Applications Note #2: "Technology Translation Applications Note", Cynthia Collart, Revision 1.0, April 13, 1989.

QUALITY ASSURANCE AND RELIABILITY

Quality Policy Statement

Vitesse believes that customer satisfaction is the only true hallmark of quality. Vitesse management and employees are committed to providing the customer with outstanding products and services. Vitesse aims for zero defects and builds quality and reliability into its products and services through excellence in design, workmanship, and statistical control methods as well as a continuous drive for improvement.

Quality Strategy

In the last decade, ever-increasing levels of integration in microelectronics have made it possible to design complex electronic systems which were once considered an impossibility. Such complex systems brought very high expectations of quality and reliability from customers.

Measurement of quality in LTPD (percent defectives) gave way to DPM (defectives per million) and lifetimes are now expressed in FITS (failures per billion hours!). In addition , modern commodity management practices such as just in time (JIT) and ship-to-stock (STS) systems stress the need for zero defects in products. To meet these expectations and to become a world class supplier, Vitesse has, from its inception, developed a very strong commitment to quality and reliability.

Vitesse perceives that excellence is achievable only through team work. Therefore, Vitesse has created a system in which quality is everyone's concern - not solely the concern of the Quality department. Vitesse has adopted a total quality control philosophy in which the Quality department serves as a facilitator and coordinator of all functions to achieve the highest levels of customer satisfaction through products and services. Figure 1 below shows the linkages of the central quality effort to all facets of the company.

The Quality department sets up systems and procedures, monitors conformance, and reports the results. Vitesse uses military standard MIL-Q-9858A as the foundation for all quality and reliability activities. Relevant portions of military standards MIL-M-38510H and MIL-STD-883C

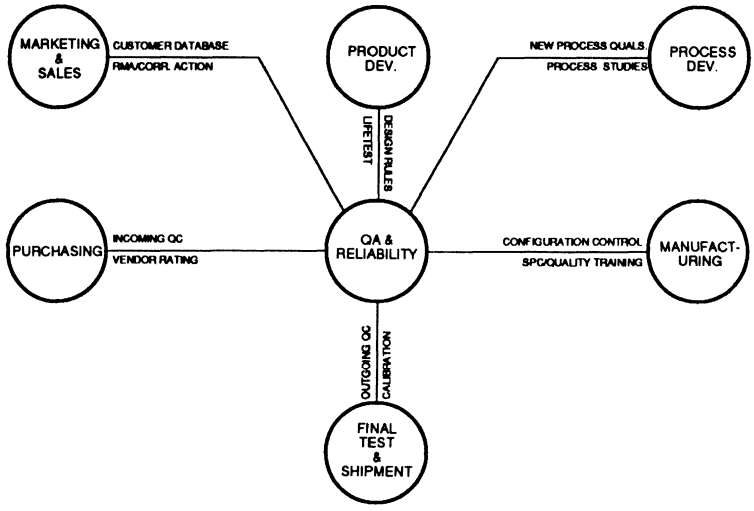


Figure 1: *Vitesse Quality Nexus*

have also been used in creating the specifications. Some of the key elements of the quality system follow.

Document Control

The manufacturing process is documented in well-defined process specifications located at each manufacturing work station. These specifications cover all processing, testing, inspection, statistical process control (SPC) and quality control procedures used in the design and manufacture of Vitesse products. All specifications are controlled, distributed and periodically audited by the Document Control section of the Quality department. Specifications are initiated, carefully monitored, and changed, if necessary, through the Engineering Change Notice (ECN) system.

Vitesse has also implemented a system to review and control customer's specifications. This system is used to compare customer requirements to Vitesse capabilities prior to quoting and accepting an order, and ultimately to translate these requirements into comprehensive lot travellers used in the wafer fab, assembly, and test areas. Individual customer requirements regarding product revision, marking, packing, labelling and shipping are handled through a customer requirements database. These two documentation systems surpass the configuration control requirements of military standard MIL-Q-9858A.

Material Quality

Final product quality is fundamentally dependent upon raw material quality. Vitesse selects vendors on the basis of their capabilities, quality history, and their willingness to support Vitesse in its drive for continuing improvement. After evaluating various vendor's materials, specifications are drawn up for the material and an approved vendor list is generated. Incoming materials are inspected to specified acceptable quality levels, any nonconformance is communicated to the vendor, and unsatisfactory materials are returned. The Quality department constantly monitors incoming material quality and corrective action taken by vendors, and a rating system has been developed to classify vendors based on the quality of their material and service. When required, the Quality department will periodically audit the vendor's quality assurance system with special attention given to the vendor's statistical control methods.

Environmental Monitoring

A controlled environment is essential to achieve low defect levels at VLSI levels of integration. Fabrication processes are carried out in a Class 10 clean room which is controlled and monitored to achieve the temperature, humidity, air velocity, and particle count specified in Federal Standard 209B. Deionized water at the point of use is also sampled continuously for resistivity (>15 Mohms) and periodically analyzed for total oxidizable carbon, silica, and bacteria counts. Assembly processes are carried out in Class 100 vertical laminar flow work stations. All work areas have conductive flooring, anti-static table tops, fully grounded equipment, and are humidity controlled to prevent static charge generation. Operators are continuously trained on ESD precautions as well as proper clean room procedures.

In-Process Inspections and Quality Gates

Figure 2 shows the process flow in the fab, assembly, and test areas. 100% production inspection and sample quality control (QC) audits have been provided at all critical process steps. QC inspections also serve as gates to hold a lot if the parameters and attributes measured at that point do not conform to the control specs.

Statistical Process Control

No one knows more about a job than the line operator who actually performs the task. Vitesse recognizes that this person, rather than the end-of-line inspector, is in the best position to improve quality. However, the operators and supervisors need empirical data to guide a change to the process.

Statistical Process Control (SPC), the legacy of Shewhart and Deming, provides this vital data. Vitesse has made a strong commitment to the use of SPC techniques to achieve very high

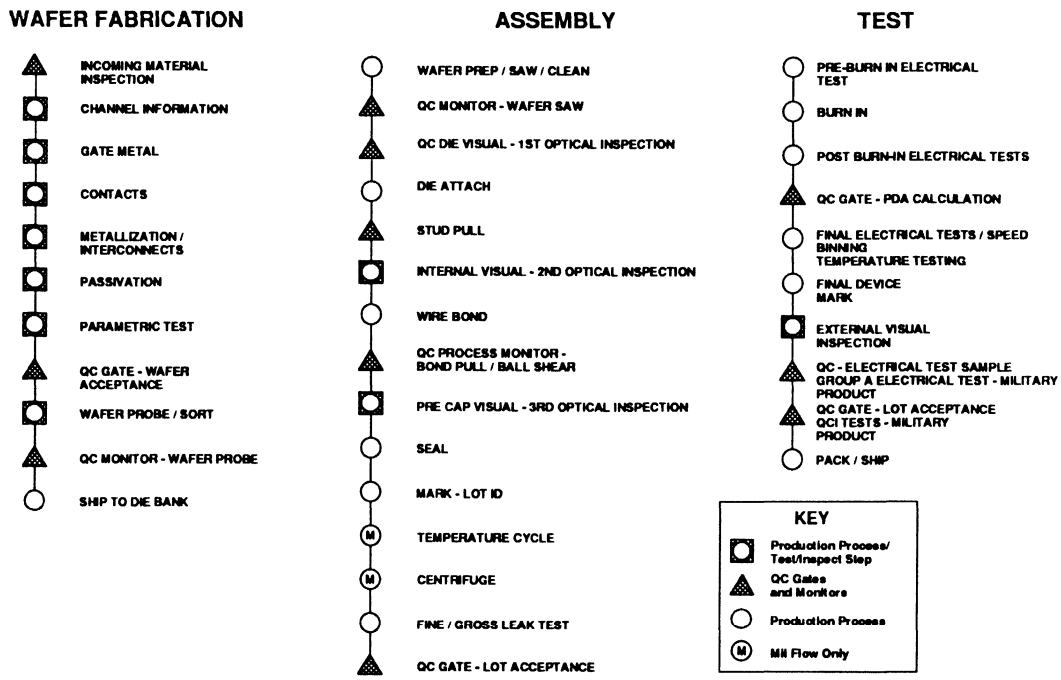


Figure 2: *General Product Flow*

levels of quality in its products.

All through the manufacturing process flow, Vitesse controls the process, rather than the product, to achieve very low defectives and very high levels of reliability. Process capability studies are conducted through Design of Experiments, before committing a new process recipe to production.

During the fabrication process, critical parameters such as metal and dielectric thicknesses, sheet resistivities, and particulate levels are measured and plotted in $\bar{X}$-R format. Process engineers constantly monitor the SPC charts and propose action for out-of-control data points. Vitesse's goal is to control most of the process steps to a minimum process capability index (C_{pk}) of 1.33, except where the parameter is limited by equipment capability or an artifact of the GaAs technology. While the entire fabrication process has as many as thirty SPC control points, ten critical steps serve as quality gates. Any lot which fails to meet the control limits is held and a Discrepant Material Report (DMR) is generated for review by quality and process engineering personnel.

In the assembly area bond-pull, bond shear, and die stud pull results are plotted and controlled by $\bar{X}$-R charts. Vitesse has also implemented FIRMS™ software to statistically process the test data obtained from Teradyne J953 VLSI tester.

A key part of Vitesse's quality strategy is to train employees in the effective use of statistics including descriptive statistics, histograms, pareto analysis, sampling, control charts, and cause and effect analysis. This strategy includes training employees in Team Problem Solving techniques and encouraging the effective use of teams to solve problems.

A formal SPC Plan has been documented and implemented at Vitesse. This plan includes training of managers, engineers, and operators in Process Capability Analysis to achieve the lowest defectives per million (DPM) levels in finished products.

Calibration and Maintenance

All gauges, test equipment, and measuring instruments are periodically calibrated in conformity with military specification

MIL-C-45662, to standards traceable to the National Bureau of Standards. All process equipment is subjected to a preventive maintenance (PM) schedule to ensure consistent operation. After any maintenance shut-down, process engineers requalify and certify the process equipment before running production lots.

Outgoing QC Inspection

All outgoing products are carefully reviewed by a Quality department inspector before shipment to the customer. Lot travellers are checked to insure that all process steps have been carried out in conformance with applicable specifications. In addition, the marking, packing, and labelling requirements are verified at this time.

Corrective Action

In keeping with its effort to reach zero defects, Vitesse has set up a root-cause analysis and corrective action system. The Corrective Action Board (CAB), comprised of a team of representatives from engineering, manufacturing, and Quality, meets regularly to review non-conformance issues arising from raw material inspections, in-process inspections, and final test. Problems reported by customers as well as life test failures are also reviewed by the CAB. The CAB works with vendors and customers where applicable to define problems and derive solutions. In all cases, the solution which guarantees total customer satisfaction is the final aim. The Quality department monitors the implementation of the corrective action and reviews the results until the non-conformance is completely eliminated. Vitesse believes that only through constant monitoring to uncover problems can continuous quality improvement become a reality.

Cost of Quality System

A Cost of Quality system as a measure of quality has been recommended in the military standard MIL-Q-9858A and has been widely recognized by the industry as a true measure of quality. Aside from being an overall indicator of quality effectiveness, quality cost numbers are an important asset to the management in prioritizing the corrective action. In keeping with this trend, Vitesse has started tracking quality costs and plans to integrate this into the Management Information System (MIS) in the future. The Prevention, Appraisal and Failure Costs (Internal and External) will be monitored by the Quality department and reported to the management on a regular basis.

Reliability Assurance

Quality is the conformance of a product to a given set of specifications at some point in time. Reliability , on the other hand, is defined as the measure of the performance of a product over an extended period of time. This period is usually the intended life of the equipment under normal operation. In other words, reliability is the measure of a product's durability. Early in the evolution of ICs, reliability was a primary requirement for military and aerospace applications only. It was often achieved - somewhat erroneously - by subjecting the end product to severe environmental stresses. The Mean Time Between Failures (MTBF) is a statistical determination method developed to determine that a given lot will operate over a specific time. The MTBF was applied to the product after the completion of the initial environmental stress process.

As electronic systems grew in complexity, reliability expectations increased dramatically. Failures in 100 FITS (100 failures in one billion hours) are nowadays very common requirements for VLSI circuits. At these levels of integration, it is no longer possible to achieve high levels of reliability by screening the end product. Reliability must really be built into the product. Quality and reliability systems based on MIL-Q-9858A and MIL-M-38510H embody this concept. Vitesse has several Reliability Assurance programs, all of which are aimed at *building in* reliability to its products. The critical elements of the process technology which contribute to the very high reliability of the Vitesse VLSI circuits and the key elements of the Reliability Assurance program are explained below:

GaAs Material

Gallium Arsenide has some attractive physical properties which give it a tremendous reliability edge over silicon. As shown in Table 1, relatively lower power dissipation and lower electric fields for the same speed of operation result in fewer thermally generated defects and virtual freedom from field-induced electro-migration. The higher band gap (1.4 eV) translates to higher activation energy (≥ 1.2 eV) which in turn results in potential high reliability, high temperature operation and enhanced radiation resistance. MESFETs built in GaAs are stable at higher temperatures and have been shown to be virtually insensitive to ionic contamination and surface effects.

Vitesse Process

Building on the inherent reliability of GaAs, Vitesse has evolved a "N-MOS like" process recipe which yields high performance VLSI circuits with very high reliability. Table 2 highlights the reliability advantages of the Vitesse H-GaAs process and compares it with "traditional" GaAs approaches. It is significant to note that the Vitesse process does not suffer from the two major failure mechanisms reported for traditional GaAs ICs, namely gate metal and contact metal interactions with the GaAs substrate at elevated temperatures.

In the Au-based gate approaches, the Ga and As diffuse into and/or through the gate metal, causing the Schottky gate to sink into the channel. As the sinking occurs, the channel depth is reduced, the threshold voltage is increased and the drain current is reduced.

Vitesse's low stress, thermally stable, tungsten-based, refractory metal gate H-GaAs process does not suffer from gate metal sinking. The tungsten/GaAs interface has been subjected to temperatures of 800° C during the implant anneal with no detrimental effects. No change in this interface is expected under normal operating conditions. Refractory metal gates are also immune to electro-migration due to localized heating under high current operating conditions.

Ohmic contacts formed by traditional Au-based systems are known to degrade over time at higher temperatures, resulting in ever increasing contact resistance values. This will significantly increase the source resistance, adversely impacting the high speed performance of the circuits. Through a proprietary, non-gold ohmic contact process, Vitesse has eliminated this problem. Other features of the contact metal process are a refractory diffusion barrier, dielectric cap, and limited reaction volume. Contacts withstand more than 10 hours at high temperatures during the processing cycle and show no degradation over

Table 1: *Reliablity Advantages of GaAs over Silicon*

Characteristic	GaAs	Silicon	GaAs Advantage
Electric Field at peak electron velocity	7 kV/cm	30 kV/cm	- Lower power dissipation - Free from dielectric breakdown and field-induced electromigration
Energy Band Gap	1.4 eV	1.1 eV	- Potential high reliability - High temperature operation - Higher activation energy - Greater radiation tolerance
Device Structures	Schottky Barrier	MOS & Bipolar	- No known surface effects - Insensitive to ionic contamination - Stable at high temperature

Table 2: Reliablity Advantages of the Vitesse H-GaAs Process

	Traditional GaAs Process	VITESSE H-GaAs	VITESSE Advantage
Device Type	D-Mode and recessed E-Mode	Self-Aligned D- and E-Mode	- Greater repeatability
Gate Material	Au-Based (TiPtAu)	W-Based	- High temperature stability - Greater V_{th} control
n+ Alignment	Stepper Aligned	Self-Aligned	- Greater uniformity - Lower source resistance
Interconnect Material	Au-Based	Al-Based	- Proven VLSI interconnect - Silicon industry solutions
Interconnect Scheme	Lift off/Ion Mill or Airbridge	Etched	- Cleaner process - Proven equipment solutions

time under normal or accelerated test conditions.

Other key factors which contribute to the high reliability and yield of Vitesse devices are:

1. Fewer mask steps; double pellicle masks for all layers.
2. High quality PECVD dielectric films
3. Planarized dielectrics for excellent step coverage of metals.
4. All dry etch processes for metal and dielectric replication.
5. DC/RF magnetron sputtered metal films.
6. Aluminum interconnects with refractory metal barriers.
7. Extensive SPC tracking of the critical process steps.

Design for Reliability

Design rules, simulation models and verification/validation tools result in layouts which ensure that the performance, quality and reliability are integrated into the final product by design. Vitesse uses very conservative design rules, which have been validated for manufacturability and reliability through extensive life tests. Such "qualification" life tests are carried out whenever there is a major design rule change or when a new generation of product or technology is released. A typical design flow has the following checks aimed at building in reliability:

1. Electrical Rules Check (ERC) to check for the violation of fanout limits, open or stuck nodes, etc.
2. Design Rules Check (DRC) to check for violation of line spacings, feature dimensions etc.
3. Layout Versus Schematic (LVS) check to verify the correct functionality of the circuit by extracting a netlist from the layout and comparing it to the original netlist.

In addition, design reviews are performed throughout the design cycle to prevent any reliability problems. Vitesse employs a device physicist who evaluates the device models continuously in order to improve products and processes.

Assembly, Test and Burn-In

As a rule, the back-end assembly and test processes use state-of-the-art silicon VLSI methods aimed at producing highly reliable products. Vitesse uses multilayer, ceramic packages with integral copper-tungsten heat sinks. These packages are specially designed to preserve the signal integrity of high speed signals. The package materials, interconnect

rules and gold plating specifications fully meet the requirements of MIL-M-38510H. Further, all new packages are fully qualified prior to production use.

The assembly processes - silver glass die-attach, aluminum ultrasonic wire bond, and hermetic seal under nitrogen ambient - contribute to the reliability of the packaged devices. All packages are 100% seal tested by Helium fine leak and Fluorocarbon gross leak per Method 1014.6 of MIL-STD-883C. Parts are inspected for external visual criteria per Method 2009.6 before sending to the test area.

Packaged parts are tested in Teradyne J953 VLSI tester for DC functional/parametric and AC parametric specs. An auto calibration routine under software control results in excellent accuracy and repeatability. Correlation Samples (Golden Parts) are used to periodically check the validity of the test hardware and software. Guard bands are employed to obviate test correlation problems.

Burn-In is a proven technique for weeding out infant-mortality rejects from a lot. Vitesse carries out 100% static burn-in on all products at T_a =125° C for 48 to 96 hours. Burn-In duration is determined based on the infant mortality characterization of the product and its maturity. All Class-B military parts are subjected to 160 hours of burn-in. Post burn-in yield serves as an ongoing reliability monitor and is reviewed on every lot by product engineering and quality. The yield on production parts through burn-in is in the 99% range and has never shown any fab process related reject.

Reliability Qualification/Monitor Tests

Vitesse has also set up Qualification and Monitor reliability programs to assess and constantly improve product reliability. The major programs are:

1. Electromigration Studies
   (200° C test at high current density)
2. Process Reliability Studies
   (250° C storage test for 1000 hours)
3. Package Qualification Tests
   (Thermal evaluation & 883C screens)
4. Accelerated Life Tests
   (Static operational life, T_a=125° C)

Electromigration Studies

Electromigration studies consist of stressing special test structures at 200° C and $1x10^6$ Amperes/cm^2 current density. The resistance changes are constantly monitored and a 50% increase in resistance is considered a failure. Such studies are conducted whenever there is a significant change in the composition and/or thickness of the metal films or interlevel dielectrics. Studies conducted so far have demonstrated that the metal systems (Metal 1 and Metal 2) show 20 FITS reliability during the first five years of operation at 100° C and worst case design current of $2x10^5$ Amperes/cm^2. These figures surpass the FIT levels normally claimed for VLSI silicon circuits.

Process Reliability Studies

A process reliability study is conducted to qualify a new process or a major change . This consists of wafer level storage test at 250° C under Nitrogen ambient. The PCM patterns are tested at zero hour and at 168, 336, 500 and 1000 hours. As mentioned earlier, gate metal and contact metal systems in GaAs ICs can interact with the substrate at high temperatures. Such degradation is almost independent of the electric current through the device. Thus, process reliability tests serve to assess the gate and contact metal reliability. In addition, the drift in device parameters and the via/cross-over integrity are also assessed. As shown below, excellent results have been obtained on the process qual tests, confirming the high reliability of the Vitesse H-GaAs process.

- Cumulative FET hours: 2 million
- No catastrophic failures of FETs, VIA strings
- Minimal parametric change in I_{DSS}, V_T, etc.

Package Qualification

All new packages undergo qualification tests which include thermal resistance evaluation (θja and θjc) and mechanical/environmental screening based on Method 5005 of MIL-STD-883C. These tests, which consist of thermal

shock, temperature cycling, acceleration (centrifuge), mechanical vibration, and hermeticity tests verify the reliability of the new package as well as the die attach and wire bond interfaces. Such qualification tests are also conducted whenever the die attach, wire bond or seal materials and/or parameters are changed. Vitesse has in-house facilities for hermeticity and acceleration tests and employs DESC certified test houses to perform MIL-STD-883C screens.

Accelerated Life Test

All new product families are subjected to the accelerated life test. This consists of an operational static bias test at an ambient of 125° C. Life test samples are drawn at random from production lots and are tested and data logged at zero hour, 168, 336, 504, 840 and 1000 hours. Tables 3 & 4 show the summary of life test results. Published studies have shown that GaAs devices follow the classical Arrhenius time-temperature equations and also display the log-normal failure distribution. Accordingly, FIT rates are calculated with these assumptions. Chi-square distribution of failures at 60% confidence level has been used and a conservative activation energy of 1.2 eV has been used to translate the failures to normal operating temperatures. It is readily seen from the charts that the FIT rates are better than those of ECL ICs and compare favorably with MOS VLSI circuits of equivalent complexity.

Failure Analysis

An important component of any reliability plan is the ability to perform effective failure analysis. Even the most reliable products fail during accelerated life tests and environmental stress screens. Such failures have to be analyzed regarding failure modes and the physics of the failure mechanism must be determined to effect process and design improvements. At times, component failures also occur at a customer's site during the board and system assembly stages. In-house failure analysis equipment at Vitesse consists of high magnification visual inspection, scanning electron microscope (SEM), and microprobe facilities. These inspections are complemented by outside test laboratories capable of conducting physical analysis such as Auger and ESCA. All failures are analyzed and the results are compiled. A report is generated which contains this data and proposes the corrective action.

Electrostatic Discharge Sensitivity

All ICs, especially those with fine line geometries, are sensitive to electrostatic discharge damage at some voltage level. A large proportion of failures at the board/system level and in the field can be traced to ESD damage. While GaAs ICs are no exception

Table 3: *Life Test Summary*

PRODUCT	COMPLEXITY	PACKAGE	SAMPLE SIZE	LIFETEST HOURS T_A = 125°C	CUMULATIVE DEVICE HOURS
2900	< 500 gates	52 LDCC	293	1536	348,612
12G422T	1000 gates	22 DIP	45	1000	45,000
8001	1500 gates	52 LDCC	106	1000	106,000
4500	4500 gates	164 LDCC	40	1133	45,320
15K	15000 gates	211 PGA	60	1000	60,000
30K	30000 gates	344 LDCC	20	500	Continuing

Table 4: Failure Rate Prediction

FAMILY	SAMPLE SIZE	CUM. DEVICE HRS @ T_A = 125°C	REL REJECTS	FAILURE RATE (FITs) T_A = 70°C	T_A = 55°C
2900	293	348,612	1	29	6
422T	45	45,000	0	100	20
8001	106	106,000	1	92	18
4500	40	45,320	0	100	20
15000	60	60,000	0	75	15

NOTE: Failure rate is calculated for an upper confidence level of 60% using χ^2 distribution and activation energy of 1.2 eV.

to this rule, they are no more ESD-prone than equivalent silicon ICs. Vitesse circuits, whenever possible, incorporate protection diodes which shunt unwanted static voltages when they occur. All new product families are initially evaluated for ESD sensitivity using the human body model (Method 3015 from MIL-STD-883C). The ESD sensitivity figures for Vitesse devices are:

High speed Inputs: 500 Volts (Min.)
Other Inputs/Outputs: 1500 Volts (Min.)

To prevent ESD damage during assembly and test operations, Vitesse has implemented ESD damage control programs according to DOD-HDBK-263 and DOD-STD-1686. Customers are advised to use established ESD precautions through all stages of the product's life to achieve continued high reliability.

Radiation Resistance

Gallium Arsenide ICs are inherently more "rad hard" than silicon devices. The higher band gap, semi-insulating substrate, and MESFET device structures contribute to at least a two orders of magnitude improvement in the total dose and neutron fluence resistance. In addition the Vitesse process has the following rad-hard features:

- Interconnects on field oxide reduces photocurrents
- Buried p-layer improves transient upset performance
- Aluminum metallization provides less scatter cross-section

Results of radiation tests on Vitesse devices have confirmed the very high rad-hard features expected with GaAs ICs:

- Total dose up to 100 Mrads with no device degradation
- Neutron fluences up to $2x10^{15}$ neutrons/cm^2 with no change in gate delay

Military Products

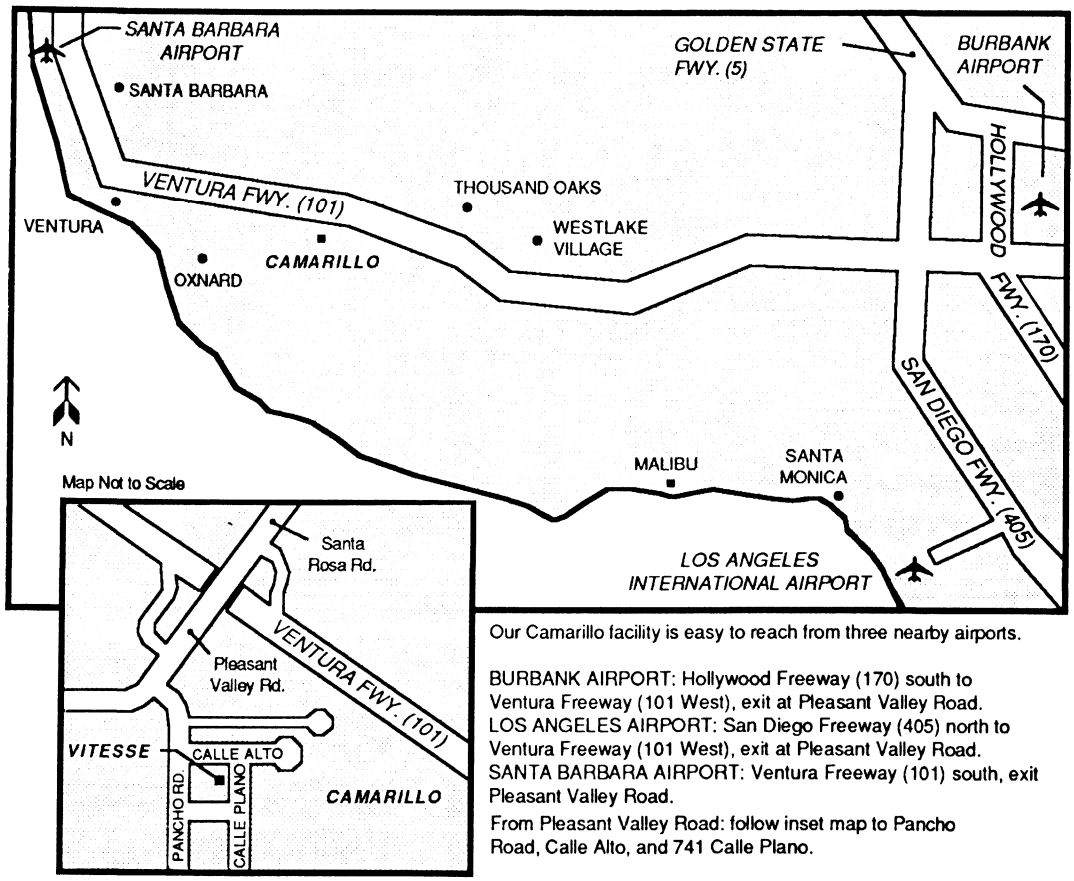
Vitesse has delivered a number of Class-B level ASICs for military applications on a non-JAN, source control drawing (SCD) basis. As shown in the product screening charts in Table 5, 100% Class-B screens in accordance with Method 5004 and Quality Conformance Inspection (QCI) per Method 5005 of MIL-STD-883C are offered for Vitesse products. Vitesse also supports Customer Source Inspection (CSI)for the military customers as required. Although the Vitesse facility is not DESC certified, the quality system incorporates most of the requirements of MIL-Q-9858A and the provisions of MIL-M-38510H. Military customers are requested to discuss their requirements with Vitesse marketing.

Table 5: Product Screening Flows

SCREEN	PROCEDURE PER METHOD 5004 OF MIL-STD-883C	COMMERCIAL / EXTENDED TEMP	MILITARY
VISUAL / MECHANICAL			
• Internal Visual	Method 2010	100%	100%
• Temperature Cycling	Method 1010, Cond C	—	100%
• Constant Acceleration	Method 2001, Cond B Y1 Orientation only	—	100%
• Hermeticity			
- Fine Leak	Method 1014	100%	100%
- Gross Leak	Method 1014	100%	100%
BURN-IN			
• Pre Burn-In Electrical	Per Applicable Device Specification	100%	100%
• Burn-In*	Method 1015, 125° C	100%	100%
• Post Burn-In Electrical	Per Applicable Device Specification	100%	100%
• Percent Defective Allowable (PDA)	Maximum PDA - 5%		
FINAL ELECTRICAL TEST			
• Static, Dynamic, Switching and Functional Tests	Method 5004, Table 1, Per Applicable Device Specification	100%	100%
QUALITY CONFORMANCE			
• Group A	Method 5005	—	Sample
• Group B	(Per Appropriate Tables	—	Sample
• Group C	for Level B Product)	—	Sample
• Group D		—	Sample
LOT ACCEPTANCE			
• External Visual	Method 2009	Sample	Sample
• Fine & Gross Leak	Method 1014	Sample	Sample
• QA Electrical	Per Applicable Device Specification	Sample	Covered by Group A Test

** Duration of burn-in for commercial products varies from 24 to 96 hours*

How to Get to VITESSE



Our Camarillo facility is easy to reach from three nearby airports.

BURBANK AIRPORT: Hollywood Freeway (170) south to Ventura Freeway (101 West), exit at Pleasant Valley Road.
LOS ANGELES AIRPORT: San Diego Freeway (405) north to Ventura Freeway (101 West), exit at Pleasant Valley Road.
SANTA BARBARA AIRPORT: Ventura Freeway (101) south, exit Pleasant Valley Road.
From Pleasant Valley Road: follow inset map to Pancho Road, Calle Alto, and 741 Calle Plano.

9

Hotel & Motel Accomodations

The following is a list of some convenient Motels and Hotels you may choose to stay in when visiting the Camarillo Headquarters of Vitesse Semiconductor Corporation.

The Holiday Inn
Tel: 805/498-6733
Hwy 101 at Ventu Park Road exit in Thousand Oaks (North)

The Days Inn
Tel: 805/375-1431
Hwy 101 at Ventu Park Road Exit in Thousand Oaks (South)

The Hyatt Westlake Plaza
Tel 805/497-9991
Hwy 101 at Westlake Boulevard in Westlake Village (South)

The Courtyard by Marriott
Tel: 805/388-1020
Hwy 101 at Santa Rosa Road in Camarillo (North)

ORDERING INFORMATION

Vitesse products are available in a variety of packages and operating ranges. The order number is formed by using a combination of the following: *Device Type, Package Type, Operating Temperature Range, Speed Option,* and *I/O Type.*

Specific ordering numbers are listed for each standard product family below and on the next page. Please consult with a Vitesse sales representative to determine device availability.

VS8000 Family - Standard Logic

VS8001 L I

Device Type

VS8001: 1.25 Gb/Sec 12:1 Multiplexer
VS8002: 1.25 Gb/Sec 1:12 Demultiplexer
VS8004: 2.5 Gb/Sec 4:1 Multiplexer
VS8005: 2.5 Gb/Sec 1:4 Demultiplexer
VS8010: SONET - 1.25 Gb/Sec 8-bit Mux/ Demux with Frame Synchronization
VS8011: SONET - 1.25 Gb/Sec 8-bit Multiplexer
VS8012: SONET - 1.25 Gb/Sec 8-bit Demultiplexer with Frame Synchronization
VS8021: SONET - 2.4 Gb/Sec 8-bit Multiplexer
VS8022: SONET - 2.4 Gb/Sec 8-bit Demultiplexer

Temperature

C: Commercial (0° to 70°C)
I: Industrial (-40° to +85°C)

Package Type

L: Leadless Chip Carrier (LCC)
F: Leaded Chip Carrier (LDCC)

VS12G00 Family - RAMs

VS12G422T L C - 5

Device Type

VS12G422T: 256 x 4-bit TTL Static RAM
VS12G478: 2K x 2-bit ECL SRAM

Speed Range

VS12G422T: 4, 5, and 6 ns
VS12G478: 5 and 6 ns

Package Type

D: 22- and 24-pin DIP
L: 28-pin Leadless Chip Carrier (LCC)
F: 28-pin Leaded Chip Carrier (LDCC)

Temperature

C: Commercial (0 to 70°C)
M: Military (-55 to +125°C) (1)

(1) Contact Vitesse for availability of military temperature range parts.

Standard Logic Evaluation Boards

VS8001 L - DUT

Device Type

VS8001/VS8002 Chip Set
VS8004/VS8005 Chip Set
VS8010/VS8011/VS8012 Series

Device Under Test

Package Type

L: Leadless Chip Carrier (LCC)
F: 28- and 52-pin Leaded Chip Carrier (LDCC)

U.S. SALES OFFICES AND REPRESENTATIVES

Corporate Headquarters

***Vitesse** Semiconductor Corporation*
741 Calle Plano
Camarillo, CA 93012 ..... (805) 388-3700
FAX: ..... (805) 388-7565

Southeastern Sales Office

***Vitesse** Semiconductor Corporation*
Palmetto Park Plaza #223
499 East Palmetto Park Road
Boca Raton, FL 33432 ..... (407) 395-1767
FAX: ..... (407) 395-1874

Northeastern Sales Offices

***Vitesse** Semiconductor Corporation*
70 Walnut Street
Wellesley, MA 02181 ..... (617) 239-8075
FAX: ..... (617) 239-8069

***Vitesse** Semiconductor Corporation*
P.O. Box 808
Chester, NJ 07930-0808 ..... (908) 879-8066
FAX: ..... (908) 879-8944

Mid-America Sales Office

***Vitesse** Semiconductor Corporation*
3010 LBJ Freeway #1281
Dallas, TX 75234 ..... (214) 888-6081
FAX: ..... (214)919-6181

Southwestern Sales Office

***Vitesse** Semiconductor Corporation*
1901 Avenue of the Stars
Suite 1774
Los Angeles, CA 90067 ..... (213) 551-1003
FAX: ..... (213) 551-0665

Northwestern Sales Office

***Vitesse** Semiconductor Corporation*
470 A Lakeside Drive
Sunnyvale, CA 94086..... (408) 245-9393
FAX: ..... (408) 245-9406

U.S. REGIONAL SALES

ARIZONA

Reptronix, Ltd.
4625 S. Lakeshore Drive
Tempe, AZ 85282-7127 ..... (602) 345-4580
FAX: ..... (602) 345-4587

CALIFORNIA

Bestronics of San Diego, Inc.
9683 Tierra Grande Street, #102
San Diego, CA 92126 ..... (619) 693-1111
FAX: ..... (619) 693-1963

Leading Concept Technologies
3700 Campus Drive
Newport Beach, CA 92660 .... (714) 851-0654
FAX: ..... (714) 851-1004

COLORADO

Thorson Rocky Mountain, Inc.
384 Inverness Drive S., #201
Englewood, CO 80112..... (303) 799-3435
FAX: ..... (303) 799-3441

CONNECTICUT, NEW YORK, NEW JERSEY

Robert Diamond, Inc.
56 Harrison Street
New Rochelle, NY 10801 ..... (914) 632-2828
FAX: ..... (914) 632-7464

ILLINOIS, WISCONSIN

Oasis Sales Corporation
1101 Tonne Road
Elk Grove Village, IL 60007 .... (708) 640-1850
FAX: ..... (708) 640-9423

INDIANA
C.C. Electro Sales, Inc.
1843 N. Meridian Street
Indianapolis, IN 46202 ..... (317) 921-5000
FAX: ..... (317) 921-5005

MARYLAND, VIRGINIA, WASHINGTON D.C.
Avtek Associates
9051 Red Branch Road
Columbia, MD 21045-2103 ..... (301) 740-5100
FAX: ..... (301) 740-5103

NEW JERSEY, DELAWARE, PENNSYLVANIA
TAI Corporation
214 Flynn Avenue
Moorestown, NJ 08057 ..... (609) 778-5353
FAX: ..... (609) 778-7828

NEW MEXICO
Reptronix, Ltd.
237C Eubank Boulevard NE
Albuquerque, NM 87123 ..... (505) 292-1718
FAX: ..... (505) 299-1611

OHIO, KENTUCKY, WEST VIRGINA, PENNYSLVANIA
Lyons Corporation
4812 Frederick Pike, #101
Dayton, OH 45414 ..... (513) 278-0714
FAX: ..... (513) 278-3609

UTAH, IDAHO
Thorson Rocky Mountain, Inc.
2309 S. Redwood Road, Suite A
Salt Lake City, UT 84119 ..... (801) 973-7969
FAX: ..... (801) 972-2484

WASHINGTON, BRITISH COLUMBIA, IDAHO
WES-TEK
13400 Northup Way, #14
Bellevue, WA 98009 ..... (206) 641-3900
FAX: ..... (206) 641-5829

U.S. DISTRIBUTOR

Nu-Horizons (Headquarters)
6000 New Horizons
Amityville, NY 11701 ..... (516) 226-6000
FAX: ..... (516) 226-6262

INTERNATIONAL REPRESENTATIVES AND DISTRIBUTORS

CANADA

Har-Tech Electronics, Ltd.
5000 Dufferin Street, #216
Downsview, Ontario
Canada M3H 5T5 ..... (416) 665-7773
FAX: ..... (416) 665-7290

Har-Tech Electronics, Ltd.
1 Bonner Street
Nepean, Ontario
Canada K2H 7S9 ..... (613) 726-9410
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